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This technical report has been reviewed and is approved for publication.

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13. ABSTRACT

The United States Air Force contracted TRW Avionics Systems Division (ASD) to be the lead in defining, developing, and documenting an Industrial Base Pilot (IBP) for producing Military Products on a Commercial Line (MPCL). This pilot program was intended to encourage the use of commercial facilities to produce military products. It has also led the way in attaining the government's goal of providing military products at half the current cost.

This document reports on the tasks performed by the IBP-MPCL Process Technology (PT) Integrated Product Team (IPT) for the program.

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Business Policies & Practices, RAH-66, F-22, CNI Line Replaceable Modules (LRMs), Manufacturing Infrastructure, Electronics, Communication ECM, Attack & Fighter Aircraft, Manufacturing & Industrial Engineering, Electrical & Electronic Equipment, Navigation Detection & Countermeasures.

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Contents

1.0 EXECUTIVE SUMMARY **1**

2.0 PROGRAM OVERVIEW **5**

2.1 PURPOSE 5
2.2 TASK OUTLINE 5
2.3 TECHNICAL GOALS 6

3.0 PHASE I EFFORT **9**

3.1 IBP-MPCL CANDIDATE MODULE SELECTION 9
3.1.1 Overview *9*
3.1.2 Selection Criteria *9*
3.1.3 Universe of Candidate Modules *10*
3.1.4 Selected Modules *10*
3.2 MILITARY VERSUS AUTOMOTIVE MANUFACTURING 11
3.2.1 Parts *11*
3.2.2 Suppliers *13*
3.2.3 Processes *14*
3.2.4 Equipment *16*
3.3 COST BASELINE 18
3.3.1 Cost Baseline *18*
3.3.2 Commercial Cost Model *18*
3.4 TECHNOLOGY ASSESSMENT AND APPLICATION 19
3.5 DESIGN APPROACH 22
3.5.1 Design Organization *22*
3.5.1.1 Structure of Organization 22
3.5.1.2 Concurrent Product and Process Development (CPPD) 23
3.5.2 The Design Environment *25*
3.5.3 Design Approach *26*
3.5.4 Part Driven Design *27*
3.5.5 Design Scoring *29*
3.6 CONCEPTUAL DESIGN 30
3.6.1 Pass 1 Plastic Ball Grid Array (PBGA) *32*
3.6.2 Pass 2 Ceramic Ball Grid Array (CBGA) *32*
3.6.3 Pass 3 Ceramic Leaded *33*
3.6.4 Pass 4 Plastic Leaded *34*
3.6.5 Pass 5 Pin Grid Array (PGA) *35*
3.6.6 Pass 6 Chip on Board (COB) *35*
3.6.7 Conceptual Design Scoring *36*
3.7 PROCESS TECHNOLOGY PHASE I SUMMARY 43
3.7.1 Non-Recurring Costs *43*
3.7.2 Recurring Costs *44*
3.7.3 Module Weight *44*
3.7.4 Design Integrity (Durability Life) *44*
3.7.5 Design Commonality *45*
3.7.6 Design and Production Risk *45*
3.7.7 Life Cycle Cost *45*
3.7.8 AEN DFM Analysis *46*
3.7.9 Design Decision Matrix *46*

4.0 DESIGN **48**

4.1 DESIGN DOCUMENTATION 48
4.1.1 Parts Selection *48*
4.1.2 Schematics *49*

4.1.3 Part Specification Documents *50*
4.2 DESIGN DEVELOPMENT TESTING 51
4.2.1 Parts & Reliability Testing *51*
4.2.1.1 Manufacture of Test Boards 53
4.2.1.2 Experimental Procedure 55
4.2.1.3 Test Results. 56
4.2.1.3.1 CR1 56
4.2.1.3.2 CR2 57
4.2.1.4 Failure Analysis 57
4.2.1.4.1 Failure Analysis Plan 57
4.2.1.4.2 CR1 Analysis Results 57
4.2.1.4.2.1 Parts Failing After Burn-in 58
4.2.1.4.2.2 Part Failing After Autoclave 60
4.2.1.4.2.3 Part Failing After HAST 61
4.2.1.4.2.4 Parametric Test Failure 62
4.2.1.4.3 CR2 Analysis Results 63
4.2.1.4.4 Additional DPA 65
4.2.1.5 Use Environment 66
4.2.1.6 Reliability Summary 67
4.2.1.7 Reliability Conclusions 68
4.2.2 Mechanical Development Testing *69*
4.2.2.1 Characterization 69
4.2.2.1.1 CTE 69
4.2.2.1.2 Stiffness 71
4.2.2.2 Durability Testing 71
4.2.2.2.1 DOE Methodology 72
4.2.2.2.2 DOE 1 Experimental Design 74
4.2.2.2.2.1 Control Factors 74
4.2.2.2.2.2 L12 Control Factor Array 76
4.2.2.2.2.3 Noise Factors 77
4.2.2.2.3 DOE 1 Test Articles 78
4.2.2.2.4 DOE 1 Test Results by Package Style 81
4.2.2.2.4.1 TSOP32 81
4.2.2.2.4.2 JLEAD32 83
4.2.2.2.4.3 CLCC32 84
4.2.2.2.4.4 PBGA561 85
4.2.2.2.4.5 PBGA313 87
4.2.2.2.4.6 PBGA169 88
4.2.2.2.4.7 Discrete Components 90
4.2.2.2.4.8 CBGA561 90
4.2.2.2.4.9 CBGA625 92
4.2.2.2.4.10 CBGA256 94
4.2.2.2.4.11 QFP240 96
4.2.2.2.5 DOE 1 Test Results by Control Factor 96
4.2.2.2.5.1 Pad Size 96
4.2.2.2.5.2 Pad Definition. 97
4.2.2.2.5.3 Pad Plating 97
4.2.2.2.5.4 Ball Size 97
4.2.2.2.5.5 Ball Material 97
4.2.2.2.5.6 Solder Paste 97
4.2.2.2.5.7 Flux Type 97
4.2.2.2.5.8 Solder Paste Volume 98
4.2.2.2.5.9 Reflow Profile 98
4.2.2.2.5.10 Second Reflow 98
4.2.2.2.5.11 Conformal Coat 98
4.2.2.2.5.12 DOE 1 Paper Champion 98
4.2.2.2.6 DOE 2 Experimental Design 101
4.2.2.2.7 DOE 2 Thermal Cycling Test Results 104
4.2.2.2.8 DOE 2 Vibration Test Results 109
4.3 DESIGN ANALYSIS 110
4.3.1 Reliability *110*

4.3.1.1 IBP-MPCL Part Reliability Prediction 110
4.3.1.1.1 Reliability Assessment Methods 110
4.3.1.1.2 CADMP2 Software Assessment Tool 110
4.3.1.2 Part Derating 113
4.3.2 Electrical 114
4.3.2.1 Power Consumption 114
4.3.2.2 Circuit Tolerance Analysis 116
4.3.2.3 Signal Integrity Analysis 118
4.3.2.4 Decoupling Analysis 118
4.3.2.5 ASIC PIN Assignments 119
4.3.2.6 DFMEA (Design Failure Mode & Effects Analysis) 119
4.3.2.7 EMI/EEE 123
4.3.3 Mechanical 123
4.3.3.1 Weight 123
4.3.3.2 Durability Analysis 124
4.3.3.2.1 Plated Through Holes 125
4.3.3.2.2 BGAs High Cycle Fatigue 126
4.3.3.2.3 BGAs Low Cycle Fatigue 127
4.3.3.3 Thermal Analysis 128
4.3.4 Software 135
4.3.4.1 On-Module Software Updates 135
4.3.4.2 Software Framework 135
4.4 DETAILED DESIGN 136
4.4.1 Electrical Design 139
4.4.1.1 Printed Circuit Design Rules 139
4.4.1.2 Routing Rules 140
4.4.1.3 Schematics and Netlists 140
4.4.2 Mechanical 141
4.4.2.1 Module Covers 141
4.4.2.2 Thermal Planes 143
4.4.2.3 Printed Wiring Boards 145
4.4.2.3.1 Construction 145
4.4.2.3.2 Layout 148
4.4.2.4 Parts 148
4.4.2.5 Adhesives 148
4.4.2.5.1 Component 148
4.4.2.5.2 Board to Core 149
4.4.2.6 Common Components 150

5.0 MANUFACTURING 153

5.1 PARTS 153
5.1.1 ASICS 153
5.1.1.1 IBM ASICs 153
5.1.1.2 LSI Logic ASICs 154
5.1.2 Lead-forming and Tinning 155
5.1.3 Tape and Reel 155
5.2 PRODUCT DEVELOPMENT AT AEN 156
5.3 BUSINESS PLAN 157
5.3.1 Business Strategy 157
5.3.2 Base Line Situation 157
5.3.3 Proposed Method 159
5.3.4 Capital Upgrades 160
5.3.5 Acquisition Process, Source of Funds 160
5.4 PRODUCTION PROCESS DEVELOPMENT 161
5.4.1 Overview 161
5.4.1.1 PV Process Flow 161
5.4.1.2 Quality Planning 167
5.4.1.2.1 PFMEA 167
5.4.1.2.2 Control Plan 167
5.4.1.2.3 Quality Model 169

5.4.2 Printed Wire Board (PWB) Assembly Processing *170*
5.4.2.1 Component Handling 170
5.4.2.1.1 Dry Nitrogen Storage for Active Components (OP #086) 170
5.4.2.1.2 PCB and Material Identification (OP #090) 172
5.4.2.2 Screen Print Solder Paste (OP #110) 173
5.4.2.3 Topside Adhesive Dispense (Op # 115) 174
5.4.2.3.1 Top Side Adhesive Dispense 174
5.4.2.3.2 Dispense Pattern Development for PV Builds 175
5.4.2.4 Component Placement Operations 176
5.4.2.4.1 Component Placement Set-up 177
5.4.2.4.2 MV 2 or Topside Surface Mount Onsertion (OP #120) 177
5.4.2.4.3 MPA or Top Side Surface Mount (OP #123) 177
5.4.2.4.4 GSM or Fine Pitch and BGA Placement (OP #125) 178
5.4.2.4.5 GSM 20 Mil Pitch Capability 178
5.4.2.4.6 Ball Grid Array Placement 179
5.4.2.5 Topside Reflow (OP #130) 179
5.4.2.6 Inspect/Touch up solder joints (OP #135, #136) 180
5.4.2.7 Flex 3 Changeover for Operations 110 Through 130 for Dual Use Production 181
5.4.2.8 Aqueous Clean (OP #330) 181
5.4.2.9 X-Ray Sampling (OP # 376) 182
5.4.2.10 PCB Singulation (OP #420) 183
5.4.2.11 In-Circuit Test/ Boundary Scan (OP #430) 184
5.4.2.12 Rework (OPs #136, 957) 186
5.4.3 Module Assembly Processing *186*
5.4.3.1 Core Bonding 186
5.4.3.1.1 Liquid Adhesive Application (OP #442) 186
5.4.3.1.2 Mechanical PCB Assembly (OP #447) 187
5.4.3.1.3 Liquid Adhesive Cure (OP #448) 188
5.4.3.2 Mechanical Assembly and Hot Bar Process 188
5.4.3.2.1 Mechanical Assembly (OP #561) 189
5.4.3.2.2 Selective Solder / Mechanical Assembly (OP #564) 190
5.4.3.2.3 Inspect (Touch-up Bendix Connector/ Flexible Crossover (OP #575) 192
5.4.3.2.4 Coaxial Cable and Ground Lug Attachment (OP # 578, #582) 192
5.4.3.2.5 Aqueous Clean and Module Bake (OP #587 and #589) 193
5.4.3.3 Final Module Assembly 193
5.4.3.3.1 Final Mechanical Assembly and Serialize Module (OP #730) 193
5.4.3.3.2 Pack and Ship Modules (OP #730 and #990) 194
5.4.3.4 ATP and ESS Testing (OP #952, #953, #981, #982, #983) 196
5.4.3.5 Conformal Coating and Underfill 196
5.4.3.5.1 Underfill of BGAs and Cure (OP #591 and #592) 197
5.4.3.5.2 Conformal Coat Spray (OP #596) 197
5.4.3.5.3 Conformal Coat Cure (OP #597) 197
5.4.4 Process Capability *198*
5.4.4.1 Initial Capability Evaluations 198
5.4.4.2 SPC During PV Runs 198
5.4.4.3 Visual Inspection Results 199
5.4.4.4 Quality Model Predictions and PV Results 199
5.4.5 Module Level BGA Rework *200*
5.4.5.1 Process Characterization 200
5.4.5.2 Equipment 201
5.4.5.2.1 Rework Station 201
5.4.5.2.2 Modifications 201
5.4.5.3 Process Development 201
5.4.5.4 Results 202

6.0 DESIGN VALIDATION 203

6.1 MANUFACTURING VERIFICATION TESTS 203
6.1.1 Component Testing *203*
6.1.1.1 ASIC Testing 204
6.1.1.2 C31 Testing 205
6.1.1.3 Other Parts 205

6.1.1.3.1 Motorola 4 Meg SRAM (MCM6246WJ20) 205
6.1.1.3.2 IDT PLL Clock Driver (IDT74FCT88915TT70PY) 206
6.1.1.3.3 IDT FIFO (IDT72241L-35JC) 206
6.1.1.3.4 Cypress PROM (CY7C277-xxJC) 206
6.1.2 ICT *207*
6.1.3 Acceptance Testing (ATP) *209*
6.1.4 Environmental Stress Screening (ESS) *209*
6.1.5 ATP/ESS Failure and Test Set Analysis *212*
6.2 DESIGN VERIFICATION 213
6.2.1 Thermal Fatigue *214*
6.2.2 LRM Electrical Performance *215*
6.2.3 Storage Temperature *215*
6.2.4 Operating Temperature *215*
6.2.5 Humidity *216*
6.2.6 Salt Atmosphere *216*
6.2.7 Functional Shock *220*
6.2.8 Handling Shock *220*
6.2.9 Chemical / Biological Exposure *220*
6.2.10 Bonding and Grounding *221*
6.2.11 EMI *221*
6.2.12 ESD Susceptibility *223*
6.2.13 Chemical Compatibility *223*
6.2.14 Ambient Pressure *223*
6.2.15 Flammability *224*
6.2.16 Rain *224*
6.2.17 Fungus *224*
6.2.18 Sand and Dust *224*
6.2.19 Explosive Atmosphere *224*
6.2.20 Acceleration *224*
6.2.21 Vibration *225*
6.2.22 Weight *225*
6.2.23 Rack Interface *225*
6.2.24 LRM Thermal Analysis *225*
6.2.25 Electrical/Electronics Hazards *226*
6.2.26 Personnel Hazards and Safety *226*
6.2.27 Maintainability *226*
6.2.28 Interchangeability *226*
6.2.29 Workmanship *227*
6.2.30 Materials, Parts and Processes *227*
6.2.31 Finishes and Protective Treatments *228*
6.2.32 Module Marking *228*
6.2.33 Acoustic Noise *228*

7.0 PROGRAM GOAL SUMMARY 229

7.1.1 Quantitative Results *229*
7.1.2 Qualitative Results *229*

List of Figures

Figure 2.3-1 IBP-MPCL Process Technology Metrics 7
Figure 3.2.1-1 ASD Parts Selection 12
Figure 3.2.1-2 AEN Supplier Selection for Parts 13
Figure 3.2.3-1 Military Baseline Process Flow 14
Figure 3.2.3-2 Projected IBP-MPCL Process Flow 15
Figure 3.5.4-1 IBP-MPCL Parts Driven Design Approach 28
Figure 3.6.7-1 Durability Scoring Algorithm 37
Figure 3.6.7-2 Recurring Cost Algorithm 38
Figure 3.6.7-3 Life Cycle Cost 38
Figure 3.6.7-4 Commonalty 40
Figure 3.6.7-5 Weight Algorithm 40
Figure 3.6.7-6 Design for Manufacturability 42
Figure 4.1.1-1 Categories of Selected Parts for the IBP PT module builds 49
Figure 4.2.1-1 CR1 Test Board 52
Figure 4.2.1-2 CR2 Test Board 53
Figure 4.2.1.3.1-1 CR1 Test Flow 55
Figure 4.2.1.3.1-2 CR2 Test Flow 56
Figure 4.2.1.5.1-1 Failure Analysis Flow 57
Figure 4.2.1.4.2.1-1 Comparator U19, Board 5C Intermetallic Growth 59
Figure 4.2.1.4.2.2-1 Op Amp U7, Board 21A Showing Bondpad Corrosion 60
Figure 4.2.1.4.2.2-2 Op Amp Control Sample (showing no corrosion) 61
Figure 4.2.1.4.2.3-1 Comparator U19, Board 12B, Silver Dendritic Growth 62
Figure 4.2.1.4.2.4-1 20 bit Buffer U15, Board 5A, Intermetallic Growth 63
Figure 4.2.3.2.1-1 DOE Thermal Cycling Environment 73
Figure 4.2.3.2.1-1 DOE Vibration Environment 73
Figure 4.2.3.2.4-1 DOE 1 Board Design 79
Figure 4.2.3.2.4-2 PBGA169 Chain Map 80
Figure 4.2.3.2.6.1-1TSOP32 Thermal Cycling Means Analysis 83
Figure 4.2.3.2.6.3-1 CLCC32 Thermal Cycling Means Analysis 85
Figure 4.2.3.2.6.4-1PBGA561 Thermal Testing Means Analysis 86
Figure 4.2.3.2.6.4-2 PBGA561 Vibration Testing Means Analysis 87
Figure 4.2.3.2.6.5-1 PBGA313 Thermal Cycling Means Analysis 88
Figure 4.2.3.2.6.6-1 PBGA169 Thermal Cycling Mean Analysis 89
Figure 4.2.3.2.6.8-1 CBGA561 Vibration Testing Mean Analysis 92
Figure 4.2.3.2.6.9-1 CBGA625 Thermal Cycling Means Analysis 93
Figure 4.2.3.2.6.9-2 CBGA625 Vibration Testing Means Analysis 94
Figure 4.2.3.2.6.10-1 CBGA256 Thermal Cycling Means Analysis 95
Figure 4.2.3.2.6.10-2 CBGA256 Vibration Testing Means Analysis 96
Figure 4.2.2.2.8-1 DOE 2 Module Layout 104
Figure 4.2.2.8-2 First Failure Summary by Part Type 105
Figures 4.2.2.2.8-3 SNR Analysis for BT Epoxy Soft Bond Boards 106
Figure 4.2.2.2.8-4 Results of 23 mm package 106
Figure 4.2.2.2.8-5 Results of PBGA 225 Package 107
Figure 4.2.2.2.8-6 Results of PBGA 256 Package 107
Figure 4.2.2.2.8-7 Results of PBGA 313 Package 108
Figure 4.2.2.2.8-8 Results of PBGA 352 Package 108
Figure 4.3.1.1.2-1 CADMP2 Input Screen for Device Package Parameters 111
Figure 4.3.1.1.2-2 Graph for Corrosion Failure Mechanism (CADMP2) 112
Figure 4.3.1.1.2-3 Device Environment Input Summary for CADMP2 112
Figure 4.3.3.1-1 Weight Comparison from Baseline to IBP-MPCL 124
Figure 4.3.3.2.1-1 Plated thru Hole Durability vs. Plating Thickness 126
Figure 4.4-1 PNP Module, A-Side View 136
Figure 4.4.2 PNP Module, B-Side View 137
Figure 4.4-3 FEC Module, A-Side View 138

Figure 4.4-4 FEC Module, B-Side View *139*
Figure 4.4.2.1-1 IBP-MPCL Module Cover *142*
Figure 4.4.2.2-1 Thermal Plane Material Property Comparison *144*
Figure 4.4.2.2-2 IBP-MPCL Module Thermal Plane with Backplane Connector *145*
Figure 4.4.2.3.1- 1 Printed Wiring Board Array with Components Assembled *147*
Figure 4.4.2.5-1 CTE Variation with Temperature for Board Bonded to Core *150*
Figure 4.4.2.6-1 Common Components *151*
Figure 5.3.2-1 AEN Resources and Processes for Module Manufacturing *158*
Figure 5.4.1.1-1 PV Process Flow for PNP and FEC Modules *163*
Figure 5.4.1.1-2 Process Flow through Dual-Use Production and Final Assembly Flow *165*
Figure 5.4.1.1-3 Flex 3 Topside Assembly Line *166*
Figure 5.4.1.1-4 Final Assembly Area *166*
Figure 5.4.1.2.2-1 Control Plan Page for PNP and FEC Modules *168*
Figure 5.4.2.1.1-1 Recommended Time-Temperature Profile for Plastic Component Dry Bake *171*
Figure 5.4.2.3.2-1 Thermal Adhesive Dispense Pattern *176*
Figure 5.4.2.5-1 Electrovert Atmos 2000 Profile for WS609-90-M13 Solder Paste *180*
Figure 5.4.2.9-1 X-ray of BGA Connections with Shorted Solder Balls *183*
Figure 5.4.2.10-1 Panel in Routing Fixture *184*
Figure 5.4.2.11-1 Board Assembly in ICT Fixture on GenRad *185*
Figure 5.4.3.1.1-1 Board with Thermal Adhesive Applied and Thermal Core *187*
Figure 5.4.3.1.3-1 Board-core Assemblies in Vacuum Bag *188*
Figure 5.4.3.2.1-1 Connector to Core-board Assembly Alignment Fixture *190*
Figure 5.4.3.2.2-1 ToddCo Hot-bar Fixturing *191*
Figure 5.4.3.2.2-2 Hot-bar Temperature and Pressure Profile for Connector Leads *191*
Figure 5.4.3.2.2-3 Fixture Detail for Crossover Soldering *192*
Figure 5.4.3.3.1 Final Assembly Fixture for PNP and FEC Modules *194*
Figure 5.4.3.3.2-1 Anti-static Module Shipping Container *195*
Figure 5.4.3.3.2-2 Shipping Box for Modules *196*
Figure 6.1.3-1 ATP Test Stand *209*
Figure 6.1.4-1 ESS Thermal Test Set-up *210*
Figure 6.1.4-2 ESS Vibration Test Set-up *211*
Figure 6.1.5-1 ICT Example failed Print-out *213*
Figure 6.2.6-1 CR1 Board 6C, Prior to 500hour Salt Fog Test *217*
Figure 6.2.6-2 CR1, Board 6C, Post 500hour Salt Fog Test. *218*
Figure 6.2.6-3 CR1, Board 6C, Post DI Rinse, Post Salt Fog *219*
Figure 6.2.6-4 DV Core and Cover After Salt Fog Exposure *220*
Figure 6.2.11-1 Chamber Setup, High Frequency Measurements *222*
Figure 6.2.11-2 Chamber Setup, Low Frequency Measurements *222*
Figure 6.2.11-3 Comparison of Shielding Effectiveness *223*

List of Tables

Table 3.1.3-1 PT/IPT Module Selection Matrix 11
Table 3.2.4-1 Process and Equipment Differences 17
Table 3.3.2-2 PNP DTC Current Summary 19
Table 3.3.2-3 RF/FEC DTC Current Summary 19
Table 3.4-1 Technology Assessment 21
Table 3.5.1.2-1 Concurrent Product and Process Development Process 24
Table 3.5.2-1 Key IBP-MPCL Design Drivers 25
Table 3.6-1 Conceptual Design Pass Matrix 30
Table 3.6.7-1 Design Scoring Parameters 36
Table 3.7.9-1 Design Evaluation Matrix 47
Table 4.2.1.5.4-1 Package Delamination Summary 65
Table 4.2.1.7-1 Failure Rate Calculations 68
Table 4.2.2.1.1-1 CTE Measurements vs Temperature for LSI Parts 70
Table 4.2.3.1.1-2 CTE Measurements Module Substrate 71
Table 4.2.3.1.2-1 Vibration Characterization Testing of DV Hardware 71
Table 4.2.3.2.3.2-1 L12 Control Factor Array 77
Table 4.2.3.2.4-1 DOE 1 Parts List 81
Table 4.2.3.2.6.1-1TSOP32 Response Table 82
Table 4.2.3.2.6.2-1 JLead32 Response Table 84
Table 4.2.3.2.6.3-1 CLCC32 Response Table 85
Table 4.2.3.2.6.4-1 PBGA561 Response Table 86
Table 4.2.3.2.6.5-1 PBGA313 Response Table 88
Table 4.2.3.2.6.6-1 PBGA169 Response Table 89
Table 4.2.3.2.6.7-1 Discretes Response Table 90
Table 4.2.3.2.6.8-1 CBGA561 Response Table 91
Table 4.2.3.2.6.9-1 CBGA625 Response Table 93
Table 4.2.3.2.6.10-1 CBGA256 Response Table 95
Table 4.2.2.2.7.11-1 Summary of Means Analysis 100
Table 4.2.2.2.8-1 DOE 2 L4 Orthogonal Array 101
Table 4.2.2.2.8-2 DOE 2 Predicted CTE and Natural Frequency 103
Table 4.3.2.1-1 Power Consumption Analysis Summary 115
Table 4.3.2.2-1 SRAM Specification Comparison 117
Table 4.3.2.2-2 FLASH Specification Comparison 118
Table 4.3.2.6-1 Sample DFMEA 122
Table 4.3.3.1-1 Weight Comparison from Baseline to IBP-MPCL 123
Table 4.3.3.2.3-1 Fatigue Analysis Results with F Tuned to DOE #1 Data 128
Table 4.3.3.3-1 Thermal Analysis Results Summary for PNP Board A 130
Table 4.3.3.3-2 Thermal Analysis Results Summary for PNP Board B 131
Table 4.3.3.3-3 Thermal Analysis Results Summary for FEC Board A 132
Table 4.3.3.3-4 Thermal Analysis Results Summary for FEC Board B 133
Table 4.4.2.1-1 Cover Material Property Comparison 142
Table 4.4.2.2-1 Thermal Plane Material Property Comparison 144
Table 4.4.2.3.1-1 Printed Wiring Board Layer Stack-up 146
Table 4.4.2.4-1 PBGA Packages and Suppliers 148
Table 5.1.1.1-1 Summary of IBM PBGA Assembly Issues and Improvements 154
Table 5.3.4 -1 New Capital Equipment on Flex-3 160
Table 5.4.1.2.1-1 Improvement Action from PFMEA for PNP and FEC Module 167
Table 5.4.2.1.1-1 Plastic Component Floor Life Classifications 172
Table 5.4.2.2-1 Aperture Adjustment for Components with Adhesive 174
Table 5.4.2.3.2-1 Adhesive Height and Dispense Patterns 176
Table 5.4.2.7-1 Flex 3 Line Changeover Times by Operation 181
Table 5.4.2.8-1 Aqueous Clean Parameters 182
Table 5.4.4-1 Initial Critical Process Capabilities 198
Table 5.4.4.2-1 Actual Run Cpks for Critical Process per Control Plan 199

Table 5.4.4.4-1 Quality Model Predicted Defect Levels in PPM *200*
Table 5.4.5.4-1 DV Module BGA Rework by Part Type *202*
Table 6.1.2-1 ICT Test Yield PNP and FEC boards *208*
Table 6.2-1 Requirements and Verification Summary Matrix *214*
Table 6.2.11-1 Cover Configurations used for EMI Testing *221*

List of Acronyms

AEN	Automotive Electronics North America
AIAG	Automotive Industry Action Group
ASD	Avionics Systems Division
ASIC	Application Specific Integrated Circuit
ATF	Advanced Tactical Fighter
ATP	Acceptance Test Procedure
BGA	Ball Grid Array
BOM	Bill of Material
BP	Business Practices
BT	Bismaleimide Triazine
CADMP	Computer Aided Design of Microelectronic Packages
CBC	Common Bus Controller
CBGA	Ceramic Ball Grid Array
CBIU	Common Bus Interface Unit
CCM	Commercial Cost Model
CDI	Cumulative Damage Index
CDRL	Contracts Data Requirements List
CIM	Computer Integrated Manufacturing
CLCC	Ceramic Leadless Chip Carrier
CNI	Communications, Navigation and Identification
COB	Chip on Board
COTS	Commercial off the Shelf
Cp	Process Capability
Cpk	Peak Process Capability
CPPD	Concurrent Product and Process Development
CR	Component Reliability
CTE	Coefficient of Thermal Expansion
DFAR	Defense Federal Acquisition Regulation
DFM	Design for Manufacturability
DFMEA	Design Failure Modes and Effect Analysis
DI	De-Ionized
DLT	Durability Life Test
DMAD	Dual Monolithic Analog/Digital Converter
DOD	Department of Defense
DOE	Design of Experiment
DPE	Data Processing Element
DSP	Digital Signal Processing
DTC	Design to Cost
DV	Design Verification
DVT	Design Verification Test
EDX	Energy Dispersive X-Ray
EEE	Electronic and Electromagnetic Effects
EEPROM	Electrically Erasable Programmable Read Only Memory
EMD	Engineering and Manufacturing Development
EMI	ElectroMagnetic Interference
EPA	Environmental Protection Agency
ESD	Electro-Static Discharge
ESS	Environmental Stress Screening
FAR	Federal Acquisition Regulation
FEC	Front-End Controller
FIB	Focused Ion Beam
FIFO	First In, First Out Buffer
FIT	Failure unIT

FLASH	Flash Programmable and Erasable Read Only Memory
FODB	Fiber Optic Data Bus
FOTR	Fiber Optic Transmit and Receive
GFRP	Graphite Fiber Reinforced Plastic
GP3	General Practice 3
GPS	Global Positioning System
HAST	Highly Accelerated Stress Test
HTOL	High Temperature Operating Life
HWCI	Hardware Configuration Item
IAR	Integrated Avionics Rack
IBP	Industrial Base Pilot
IC	Integrated Circuit
ICT	In-Circuit Test
IFDL	Intra-Flight Data Link
IFF	Identify Friend or Foe
IMA	Integrated Microwave Assembly
IPC	Institute for Interconnecting and Packaging Electronic Circuits
IPT	Integrated Product Team
ISIR	Initial Sample Inspection Report
ISW	Initial Sample Warrant
JTAG	Joint Test Access Group
KGD	Known Good Die
KOVX	Crypto Processing Unit
LCC	Life Cycle Cost
LLSP	Low Latency Signal Processor
LMTAS	Lockheed Martin Tactical Air Systems
LRM	Line Replaceable Module
LTCC	Low Temperature Cofired Ceramic
MAME	Master Messaging ASIC
MCM	Multi-Chip Module
MI	Manufacturing Infrastructure
MPCL	Military Products from Commercial Lines
MPCM	Manufacturing Process Cost Models
MPSD	Modular Port Scan Device
MTBF	Mean Time Between Failure
MTC	Maintenance Test Controller ASIC
NBP	Narrow Band Processor
NRE	Non-Recurring Engineering
NTE	Not To Exceed
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PEAP	Pulse Environmental Angle of Arrival Processor
PEM	Plastic Encapsulated Microcircuit
PFMEA	Production Failure Modes and Effect Analysis
PGA	Pin Grid Array
PLCC	Plastic Leaded Chip Carrier
PLL	Phase Lock Loop
PM	Program Manager
PNP	Pulse Narrowband Preprocessor
PPM	Parts Per Million
PT	Process Technology
PTH	Plated Thru Hole
PV	Production Validation
PWB	Printed Wiring Board
Q	Amplification Factor
QFP	Quad Flat Pack

QM	Quality Model
RAH	Recognizance and Attack Helicopter
RAM	Random Access Memory
REM	Responsible Engineering Manger
RF	Radio Frequency
RMA	Rosin Moderately Active
RME	Responsible Manufacturing Engineer
RPN	Risk Priority Number
RTC	Real Time Clock
RTP	Receive Transmit Processor
SBIT	Startup Built in Test
SCD	Specification Control Drawing
SDF	Software Development Folders
SDP	Software Development Plan
SEM	Scanning Electron Microscope
SEM-E	Standard Electronic Module – E format
SMA	Subminiature-A connector
SMT	Surface Mount Technology
SNR	Signal to Noise Ratio
SOF	Safety of Flight
SOIC	Small Outline Integrated Circuit
SOJ	Small Outline J-Lead
SOP	Small Outline Package
SOP	Start of Production
SPC	Statistical Process Control
SQAA	Software Quality Assurance Audit
SQAP	Software Quality Assurance Plan
SRAM	Static Random Access Memory
SSOP	Shrink Small Outline Package
STE	Special Test Equipment
TDI	Thermal Damage Index
Tj	Junction Temperature
TM	Test Maintenance
TOD	Time of Day
TPI	Technical Performance Index
TSOP	Thin Small Outline Package
TSP	Time Sync Pulsing
UHF	Ultra High Frequency
V&V	Verification and Validation
VDI	Vibration Damage Index
VHF	Very High Frequency
WCC	Work Cell Controllers
WL/MT	Wright Labs/Manufacturing Technology
WS	Water Soluble

1.0 EXECUTIVE SUMMARY

The Industrial Base Pilot Military - Products from Commercial Lines (IBP-MPCL) program demonstrated the production of military electronics products on a commercial manufacturing line, showing cost reductions, improved quality and equivalent performance. The successful demonstration of this project ensures DoD of a quality manufacturing base that will be flexible enough to meet defense requirements, both routine and in emergency. TRW Avionics Systems Division (ASD), the IBP-MPCL prime contractor, has identified and overcome the barriers to building military products on commercial assembly lines. The IBP-MPCL consisted of three major tasks:

The Process Technology (PT) team designed and built military avionics hardware on a commercial assembly line at TRW Automotive Electronics Group's North America (AEN) Marshall, IL plant.

The Manufacturing Infrastructure (MI) team implemented a Computer Integrated Manufacturing (CIM) system that links ASD's engineering database with the Marshall plant's automated assembly equipment.

The Business Practices (BP) team developed commercially acceptable replacements for military specifications, standards, and contract terms to enable future joint commercial-military work.

All three teams were tasked to transfer results from the program to government and industry. This report focuses on the results of the Process Technology activities, and is a component of the technology transfer. Similar reports are published by the MI and BP teams and are referenced within. Numerous reports, papers and presentations over the duration of the program have been published and presented at Defense Manufacturing Conferences (DMCs), NAECON, Air Force ManTech Industry Days, at technical conferences and at technical interchange meetings. The process technology results are summarized here.

Results confirm that both cost and performance objectives can be met. Cost savings in the range of 50% -70% for the "commercialized designs" have been confirmed by actual procurement, assembly and test data. In addition, extensive reliability and durability testing shows that commercial parts and processes are robust enough to meet or exceed military requirements. The PT team demonstrated business practices developed under this program are serving as a model for streamlined acquisition and for implementation of a commercial alternative to Military Specifications and Standards.

The primary program goals for the PT team over the three-phase program were as follows:

Phase 1: Perform conceptual design trades for design packaging approaches (Plastic vs. ceramic and Chip on Board, vs. leaded vs. area array packages) and design rules for commercial assembly.

Phase 2: Perform detailed design and construct design validation (DV) modules in the TRW AEN plant, and to demonstrate durability and reliability of the "commercial versions" of the design.

Phase 3: Design update and build of 127 production verification units (PV) in the Automotive plant, demonstrating a 15 minute line conversion and implementation of the BP team recommendations.

These goals have all been achieved.

In the conceptual design phase of the program, concerted effort was spent assimilating TRW AEN design for manufacturing rules and requests into the TRW ASD design infrastructure. Design candidates were quantitatively scored in decision matrix methodology and the manufacturing line was selected.

In the detail design phase of the program, risks identified under the conceptual design phase were analyzed or tested. New filter circuitry using commercial components was analyzed and breadboarded. Durability testing of the Plastic Ball Grid Array (PBGA) package solder joints was performed, and exhaustive reliability testing of commercial off the shelf (COTS) plastic encapsulated microcircuits (PEMs) and commercially packaged ASICs were performed. Sixty (60) DV units of two types, (30) each, were produced to verify the detailed design and manufacturing processes.

In the last phase of the program, the detailed designs were updated to fix shortcomings identified by the DV unit builds and 127 PV units were built. These units were exposed to the full battery of tests used on the Military version predecessors: Design Verification Tests (DVT), Acceptance Tests (ATP), Environmental Stress Screening (ESS), Durability Life Tests (DLT), and other Verification and Validation Tests (V&V) at the module level. DV and PV units have also been placed into next higher assemblies, aircraft racks, and continue to experience rack tests.

By the end of 1999, IBP-MPCL modules will have been through rack safety of flight (SOF) and be deployed for EMD aircraft integration.

The results of these activities have demonstrated a 48% cost reduction on one module and a 68% reduction on the second module. The module weights have been reduced by 35%. Durability testing indicates that at least 1 full 20-year lifetime of military fighter environments can be achieved utilizing commercial parts and processes. Component reliability far in excess of mission life has been demonstrated by accelerated tests. Full

functional compatibility with the predecessor military module has been verified by DVT.

2.0 PROGRAM OVERVIEW

The United States Air Force contracted TRW Avionics Systems Division (ASD) to be the lead in defining, developing, and documenting an Industrial Base Pilot (IBP) for producing Military Products on a Commercial Line (MPCL). This pilot program was intended to encourage the use of commercial facilities to produce military products. It has also led the way in attaining the government's goal of providing military products at half the current cost.

This document reports on the tasks performed by the IBP-MPCL Process Technology (PT) Integrated Product Team (IPT) for the program.

2.1 Purpose

The IBP-MPCL PT team mission was to modify selected military module designs for compatibility with commercial processes; demonstrate dual-use manufacturing capability; validate business practices and manufacturing infrastructure changes, while improving quality and reducing costs. In addition to this mission, supporting documentation was created to effect a transfer of technologies to other DOD programs.

2.2 Task Outline

The Phase 1 task for the Process Technology (PT) Integrated Product Team (IPT) included:

- Definition of the purpose and technical goals listed here.
- Selection of the detailed designs to include/exclude from this program. Detailed comparison of the methods (parts, materials, processes and equipment) utilized at both the Military and the Commercial facilities
- Detailed cost baseline to understand the distribution of costs for the selected designs.
- Technical assessment of emerging processes to support the generation of detailed conceptual design, and supporting analysis.
- Scoring and selection of the best conceptual design to pursue for Phase 2.

The Phase 2 tasks for the Process Technology Team included:

- Detailed redesign of the selected LRMs for use of the automotive electronics production process.
- Simulation of the design and analysis of the durability of the design.

- Planning the production of Design Validation Units at the automotive facility.
- Generation of detailed process flows and work instructions.
- Implementation of new capital equipment.
- Procurement of the BOM and production of 30 units each of the two selected LRMs.
- Validation of component reliability, durability analysis, functional test, ESS, DLT and System use of the DV LRMs.
- Development and transmission of metrics to quantify and measure the benefits of the approach, and presentation of the metrics to the customer.

The Phase 3 tasks for the Process Technology Team included:

- Implementation of corrections and improvements into the Phase 2 DV designs.
- Conduction of a production validation run of at least 116 units total of the two LRM configurations, and demonstration of a maximum change-over at each station of 15 minutes or less.
- Performance of validation tests on the resulting production modules to validate the ease of manufacture and the product robustness. Testing to include ESS, functional, DLT and IAR tests.
- Delivery of 77 LRMs to the customer for transfer to the customer.

2.3 Technical Goals

In order to provide an objective measure of IBP-MPCL program achievement of technical goals, it was determined that a uniform measure of technical performance was required. It was desired to use a quantitative measure that could also function as a gauge of progress towards meeting those goals. To this end, a table of critical parameters was established, with weighted scores tabulated and normalized to an index of 100%. This score, or Technical Performance Index (TPI), was updated and monitored as the program progressed. Critical parameters used for the TPI matrix are listed in Figure 2.3-1. As can be determined by study of the matrix, technical success is based upon interchangeability and/or interoperability with military modules. A brief description of some of the critical parameters follows.

Metric	Methodology	Target (Basis)	Results	Index
PNP Cost	Mat'l – Actuals Labor - Estimates	$18.0k (50% Reduction)	$18.6k	97%
FEC Cost	Mat'l – Actuals Labor – Estimates	$17.4k (50% Reduction)	$11.0k	100%
CDI (Durability / Reliability)	Test	1.0 (1 Life)	1.0	100%
Form, Fit, Function	Demonstration	100% (Military Comparison)	100%	100%
Weight	Test	1.3 Lbs (Military Baseline)	1.0 Lbs	100%
# of Processes with Cpk > 1.33	Build	14 (DFM Analysis)	11	79%
# of Processes with Set-up Time < 15 Minutes	Demonstration	11 (ROAE Analysis)	11	100%
			TPI	97%

Figure 2.3-1 IBP-MPCL Process Technology Metrics

Weight - The weight goal is based upon the current module design.

Cost - The cost goal is based upon current module allocation, adjusted and modified to the Design to Cost (DTC) model.

Durability Life - The durability life goal is based upon current module requirements. Durability life can be defined as the life expectancy for product performance without design controllable failures due to high and low cycle fatigue and corrosion.

Form Fit and Function – Goal is 100% equivalence to current module.

CPK - Process variables must have a measured, minimum statistical process repeatability and accuracy (Cp & Cpk) to meet program goals and be compatible with the AEN factory.

Setup Time - Minimal setup time (time required to convert the automotive production line to Military product) is essential to maintain viability of the Dual-Use concept.

3.0 PHASE I EFFORT

3.1 IBP-MPCL Candidate Module Selection

3.1.1 Overview

The IBP-MPCL program was required to recommend three or more candidate electronic LRM/PCAs from aerospace weapon systems for this program. A minimum of two candidate LRM/PCAs were to be selected for demonstration in the program. The selection criteria were based upon applicability to commercial production processes and facilities. Recommended modules included the Pulse/Narrowband Processor (PNP), CNI Bus Coupler (CBC), RF Front-End Controller (RF/FEC), and the Low Latency Signal Processor (LLSP). The modules that were recommended for demonstration were the PNP and RF/FEC.

3.1.2 Selection Criteria

Design and Manufacturing representatives, from TRW Avionics Systems Division (ASD) and Automotive Electronics North America (AEN), collectively determined a module selection criteria list. The selection criteria for the modules follows:

• Commonality among Weapons Platforms - The PT IPT determined this was an important criterion in order to ensure broad applicability and critique of program results.

• Multiple Use Within Systems - This is a criterion because of significant leverage to be gained by increased production quantities of modules.

• High Design-To-Cost - Higher cost items provide the most opportunity to realize the benefits of the IBP-MPCL program.

• SEM-E Module Construction - Physical configuration of the hardware is most critical to the success of utilizing the AEN manufacturing line for the IBP-MPCL selected modules. The SEM-E configuration provides sufficient compatibility with the automated assembly lines at AEN to utilize an optimum number of existing processes and equipment.

• Automation Compatibility - In order to utilize the AEN manufacturing line with the minimum amount of disruption and off-line processes, the selected modules must be configurable with materials, components, equipment, and processes suitable for high-levels of automation. The module design must also afford quick changeover from commercial hardware/processes to military hardware/processes. In addition to design

and material compatibility with automation, the hardware must meet physical limitations of the equipment that includes:

– Component dimensions NTE 2" X 2"

– Board dimensions NTE 250mm X 350mm X 2.5mm

• Digital/Analog Circuitry - The materials, processes, equipment, and staff at AEN are oriented towards digital and analog circuits and systems. Conversely, capability is minimal at AEN with RF hardware, backplanes, apertures, etc. The selected modules needed to be compatible with AEN capability.

• Common ASD/AEN Component Suppliers - In order to optimize the benefits of commercial procurement, the selected modules should contain an optimum number of components that are also available from suppliers that have commercial contracts with AEN.

3.1.3 Universe of Candidate Modules

Modules for consideration were identified from military platforms. The universe list was summarily reduced to a subset list based upon parameters that precluded inclusion in the weighted scoring matrix used to rank candidates for selection. Rejected from initial consideration were those functions that were not modular, and/or were obviously specialty items such as power supplies, apertures, etc., as well as items that are essentially RF. Also rejected were modules which were not defined (e.g. early in the design cycle) to the extent that selection criteria could be applied with reasonable certainty. Other modules rejected were modules clearly incompatible with the AEN factory. This resulted in a compiled list of candidates.

3.1.4 Selected Modules

The PNP, LLSP, and RF/FEC are utilized on multiple military platforms. These three modules also meet much of the selection criteria listed above. Of the remaining, only the CBC meets sufficient selection criteria. Subsequently, those four modules were considered viable for IBP-MPCL program utilization. Of the four, the two modules selected for demonstration were the PNP and the RF/FEC. The selection categories, weightings, and the culled module selection list with ranking scores are presented in Table 3.1.3-1. Attributes were identified and weighted in the selection matrix, with points attributed for commonality, compatibility with AEN processes, rate of application and leverage on DTC.

Table 3.1.3-1 PT/IPT Module Selection Matrix

Category	Commanality Among Platforms	Digital/Analog	SeEM-E Size Does Not Exced 250mmX250mm	Automated Assembly	Compatible Processes	PWB Thickness Preferred Component Size 50 mmX 50mm	Used in Multiple Places per System	High DTC Item	Common Component Supplier	Changeover Time	
Weighting Factor/Multiplier	5	5	2	3	2	3	4	4	5	2	
Modules Options											**Total**
MOPS	1	5	8	4	8	4	1	5	2	5	130
PNP	7	8	8	8	8	8	6	8	8	8	267
RF/FEC	8	6	8	7	8	7	7	7	6	6	242
+5V Power Sup	6	3	8	1	8	2	5	1	1	1	117
UHF/VHF Rec	4	2	8	3	8	3	4	4	5	4	145
GPS Rec/Proc	3	1	8	5	8	5	3	2	4	3	128
USP	2	4	8	2	8	1	2	3	3	2	110
CBC	5	7	8	6	8	6	8	6	7	7	225

3.2 Military Versus Automotive Manufacturing

There are a number of differences between ASD and AEN manufacturing which must be identified and resolved in order to ascertain successful transition of the module into an industrial manufacturing facility. The following sections on parts, suppliers, processes, and equipment discuss the identification and analysis of differences in technology, which affect the design and/or manufacture of the IBP-MPCL version of the selected modules.

3.2.1 Parts

Figure 3.2.1-1 depicts the baseline (1994) ASD process flow for the selection of defense contract parts. It is based upon government furnished baseline established by the Defense Logistics Agency. Deviations from this baseline require contractor and Parts Control Board approval. Figure 3.2.1-2 shows the contrasting process for parts selection and approval at AEN. This is a typical automotive industry parts selection process, which is primarily supplier driven. That is, each supplier to AEN is required to comply with an internal approval and certification process prior to acceptance, but are otherwise left to their own resources as to how to best meet user requirements.

In addition to these differences, the majority of the active microcircuits for ASD are hermetically packaged (typically ceramic or metal) and have a specified operating temperature range of -55°C to +125°C. AEN microcircuits are typically less complex, encased in non-hermetic packages (plastic molding compound), and are specified to operate over either the industrial temperature range of -40°C to +85°C or the automotive temperature range of -40°C to +125°C.

Passive components such as resistors, capacitors and inductors for ASD military programs traditionally have established reliability ratings and derating factors imposed through military specifications. AEN selects passive devices to meet specific application operating conditions and required environments, rather than a general specification.

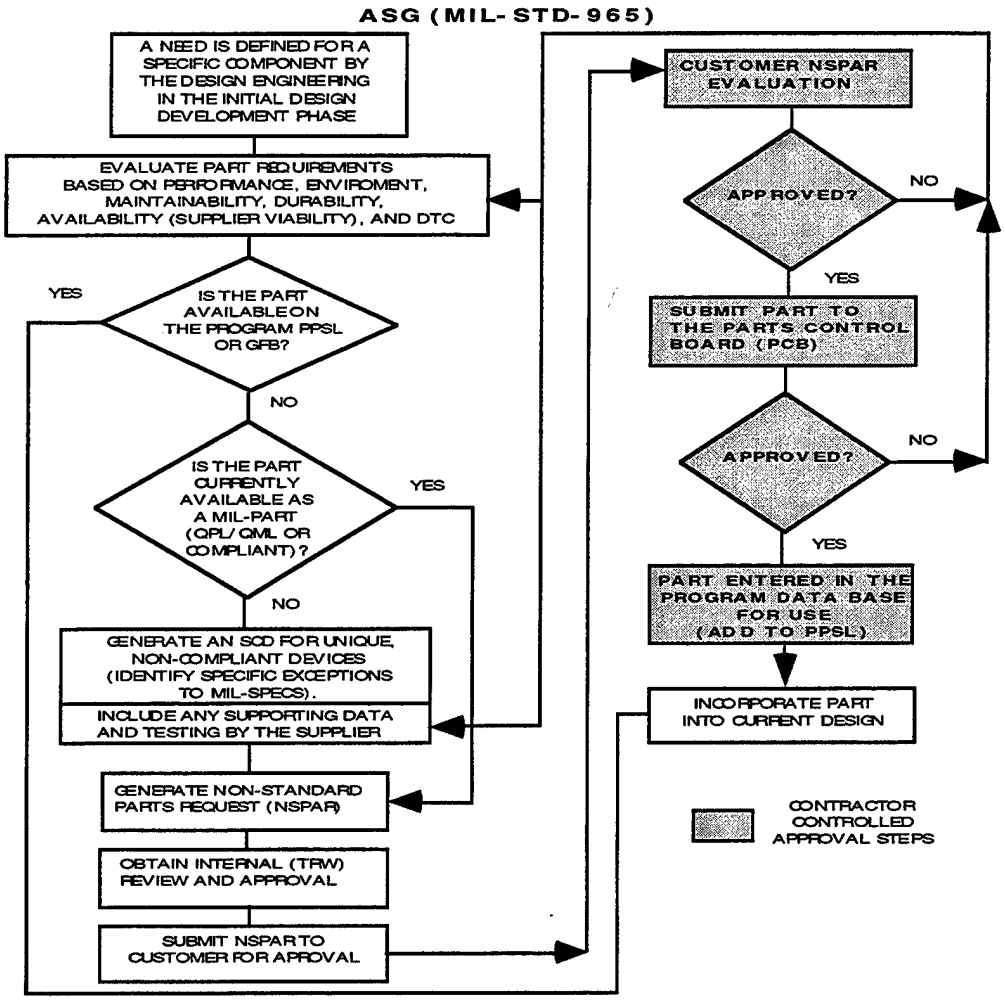

Figure 3.2.1-1 ASD Parts Selection

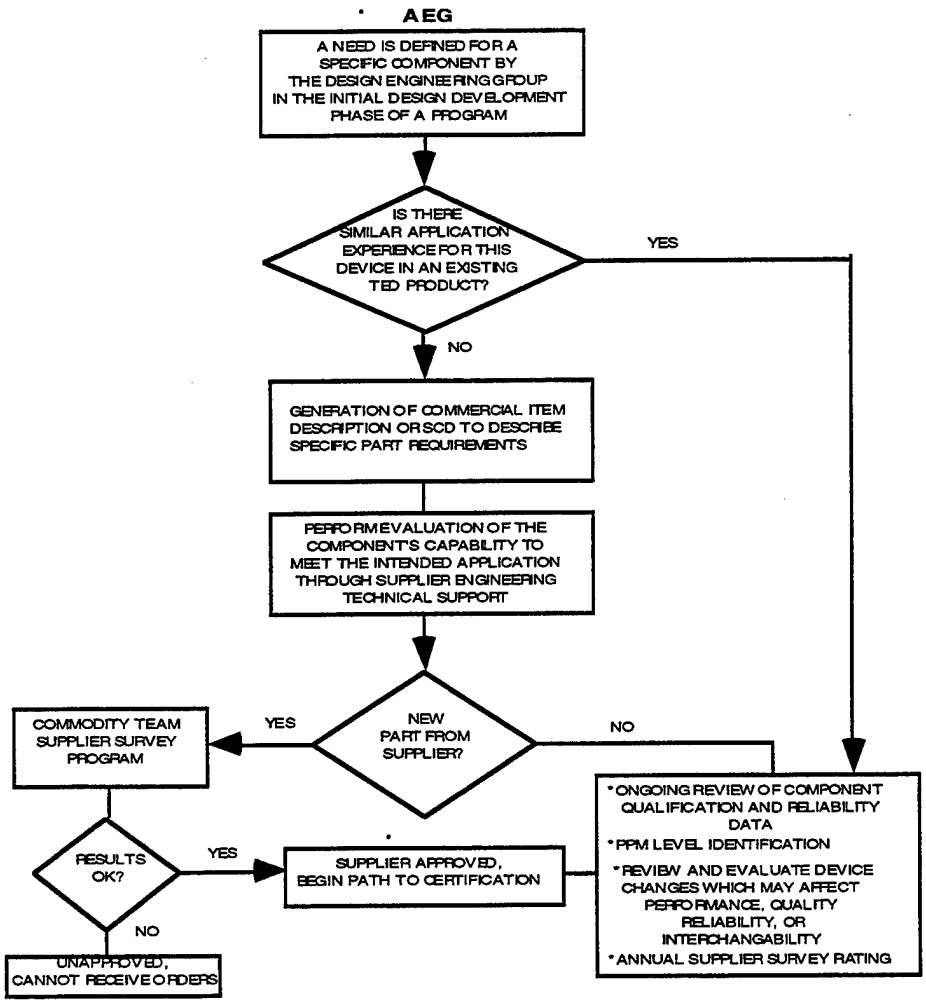

Figure 3.2.1-2 AEN Supplier Selection for Parts

3.2.2 Suppliers

Suppler selection by AEN is a comprehensive and ongoing process to develop a base of approved and certified suppliers by initially surveying each supplier through commodity teams and continuing to develop these selected suppliers through demonstrated cost improvement and achieved PPM certification levels.

ASD establishes approved part suppliers based on those companies that can supply components approved to military specifications and operate according to approved military standards and practices.

3.2.3 Processes

The manufacturing flow for the military modules has 24 major process steps. It was evident from process analysis that opportunities for manufacturing cost reduction afforded by transition from the ASD factory to the AEN factory were twofold: Reduce the number of process steps, and resolve (by design or process modification) the differences in requisite processes. Figure 3.2.3-1 is a depiction of the military baseline process flow. Figure 3.2.3-2 is a depiction of the projected IBP-MPCL process flow.

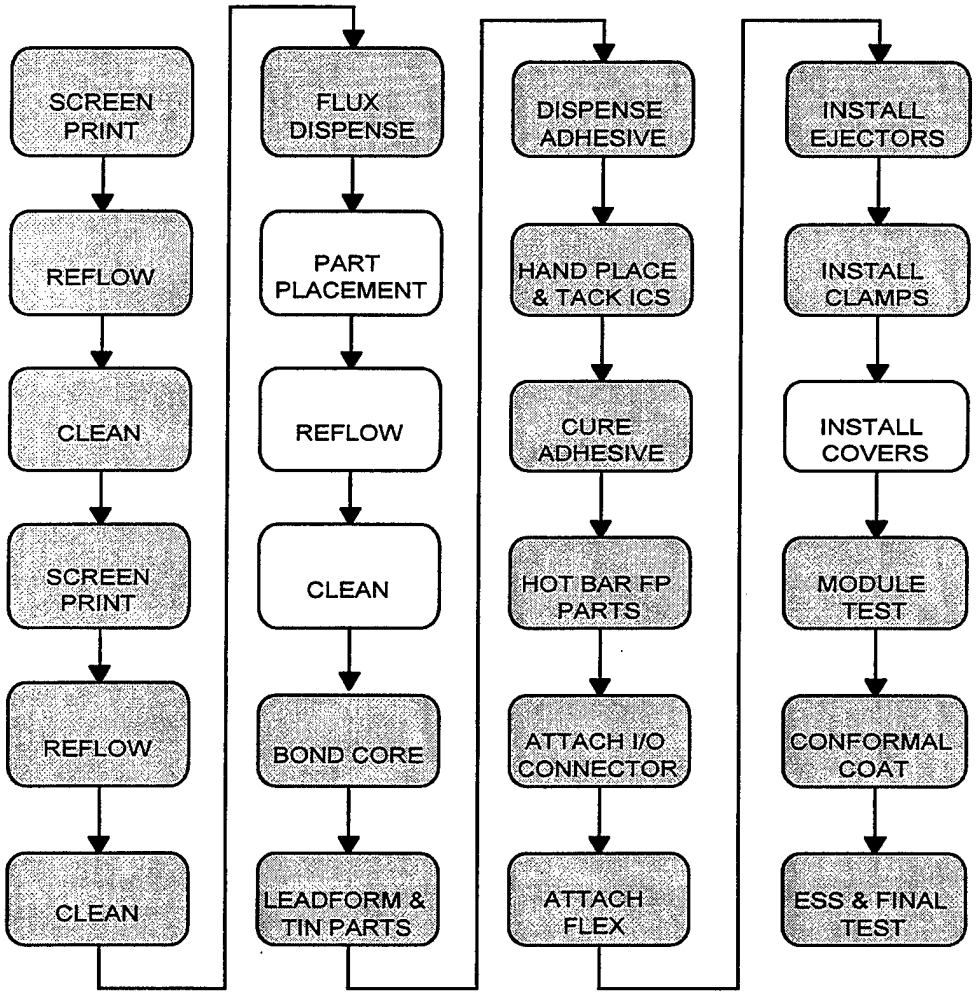

Figure 3.2.3-1 Military Baseline Process Flow

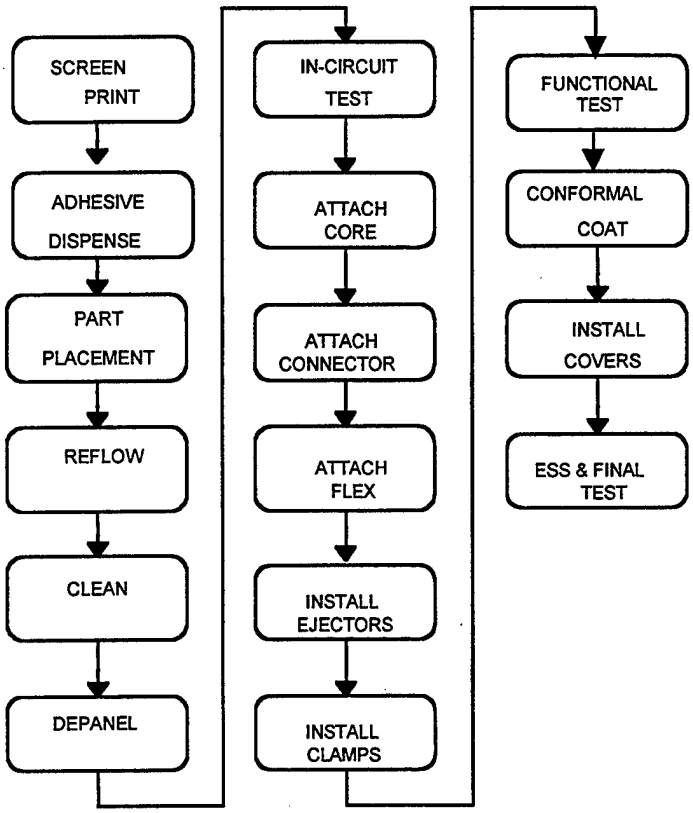

Figure 3.2.3-2 Projected IBP-MPCL Process Flow

The IBP-MPCL Process flow diagram shows 5 processes for which a current AEN process did not exist. Processes had to be installed at AEN to accommodate these differences. Process modifications required were:

a) Connector Attach. Hot bar solder reflow processes required.

b) Crossover Flex Attach. Hot bar solder reflow processes required.

c) Module Ejector Installation. Fixturing or hand assembly should be obviated.

d) Module Clamp Installation. Fixturing or hand assembly should be obviated.

e) Environmental Stress Screening (ESS) & Final test. Special Test Equipment (STE) or alternative test hardware/software required.

3.2.4 Equipment

Process requirements that cannot be accommodated with existing equipment necessitate elimination or modification of the process and/or modification or replacement of the equipment. In the case of the IBP-MPCL baseline module, there are few notable differences in required equipment, which remain after process elimination/modification options have been explored. The following are equipment related issues that were addressed.

a) Custom lead forming and tinning. In the case of leaded devices, the IBP-MPCL baseline module has considerably more leads of higher density and finer pitch than could be accommodated on AEN equipment.

b) Core bonding. This process did not exist at AEN and was developed as an off-line operation.

c) Thermal adhesive dispense underneath active components. Initial equipment at AEN could perform this process, but the equipment was not located at the appropriate place in the assembly line.

d) Hot bar reflow. Crossovers and connectors require mass lead termination or other means to perform precision placement and solder reflow. Equipment for this process did not exist at AEN.

e) Functional module test. The IBP-MPCL modules are considerably more complex and require substantially more test vectors than can be accommodated by initial equipment at AEN.

A summary table of process and equipment differences is presented in Table 3.2.4-1.

Table 3.2.4-1 Process and Equipment Differences

ASD Process	AEN Process	Impact	Actions
White Ink Rupper Stamp Marking	Kapton Barcode Label Marking	MIL Standard not used by AEN	Use Kapton Barcode labels with AEN symbology
Clean Incoming PCBs	No Incoming PCB Cleaning	Additional Batch Process and Handling	Eliminate Incoming PCB Clean
Double Screenprint, Reflow and Clean Process for LCC packages	Single Screenprint, Reflow and Clean Process	Cycle time and labor adder of 20 minutes. Batch process flow and handling.	Replace LCC packages with commercial leaded packages
Paste Flux Dispense	No equivalent Process	Cycle time and labor adder. Dispensing equipment not available. Off-line process for AEN	Replace LCC packages with commercial leaded packages
Core Bonding	No equivalent Process	Cycle time adder of 4 hours per 5 modules. Labor adder of 1.5 hrs per module. Process flow and handling equipment not used by AEN	Evaluate: pre-bond PCB Mechanical Attach Solder bonding Improve Process Subcontract Process
Lead form and tin components	Components formed and tinned by supplier	Labor adder for lead form and tinning. Equipment and processes not used bye AEN	Supplier to perform lead form and tin
Dispense and cure adhesive for ASIC/MCM thermal and mechanical bonding	High viscosity liquid dispensing process for RTV	Liquid process are being eliminated by AEN. In-line process at SMT not used by AEN. Positive displacement equipment not available.	Evaluate: BGA repackaging Elimination of Adhesive Alternative matl
Manual ASIC/MCM placement and tack soldering	No equivalent Process	Cycle time and labor adder of 24 minutes per module. Batch process flow and handling	Use reflow compatible packages, Upgrade placement machine for large packages.
Hot Bar reflow of ASIC/MCM Packages	No equivalent Process	Cycle time and labor adder of 48 minutes per module. Lower process quality. Batch process flow and handling. Equipment and process not used by AEN	Use reflow compatible packages. Upgrade placement machine for large packages.
Align, Hot Bar reflow and excise I/O connector	No equivalent Process	Cycle time and labor adder of 12 minutes per module. Batch process flow and handling. Equipment and process not used by AEN.	Restraint: Connector mating not to be changed. Evaluate: Alternative connector attach styles Hot gas soldering
Align, Hot Bar reflow and excise I/O Crossover	No equivalent Process	Cycle time and labor adder of 12 minutes per module. Batch process flow and handling. Equipment and process not used by AEN.	Evaluate: Rigid-flex PCBs Flex Xover in Conn Through hole PCB Hot gas soldering
Install ejector levers, wedge clamps, pin guide and covers	No equivalent process for pin guide ejectors and wedge clamps. Automated manual screwdriving.	Cycle time and labor adder of 10 minutes per module. Batch process flow and handling. 2 screw types require additional tooling	Evaluate: Cover redesign Solder covers Integral clamp at rails Redesign ejector Standardize screws Reduce fastener qty. Snap fit design Subcontract Assy
Module Test	In-Circuit test	IBP-MPCL modules require clock speeds and capabilities not currently available at AEN	Adapt in-circuit hardware to test SBIT at speed. Use JTAG to run test at a lower speed.
Parylene conformal coat	Acrylic dip and spray coating, evaluating silicone coating.	Cycle time and labor adder. Batch process flow and handling. Equipment and process not used by AEN.	Evaluate alternative coating materials eliminate conformal coat subcontract conformal coat
ESS Test	Batch and flow-through ESS	High system cost and support restraint.	Evaluate reducing IBP-MPCL ESS testing to match AEN capability. Perform ESS testing at ASD
Final Test	Accelerometer and parametric test	High system cost and support restraint.	Implement final test system at AEN Perform ATP at ASD

3.3 Cost Baseline

3.3.1 Cost Baseline

The military Engineering Manufacturing Development (EMD) program has established very specific parameters for calculating the cost baseline and the current production cost estimates. These costs are based upon specific defined criteria such as combined ship-set procurement quantity (442), constant 1990-dollar value, material escalation formulas, learning curves, etc. The military DTC algorithm is cumbersome to the AEN commercial operating environment. For the convenience of readily calculating DTC for the purpose of the IBP-MPCL program, a Commercial Cost Model is utilized.

3.3.2 Commercial Cost Model

The difference between the military and the Commercial Cost Model (CCM) is listed in Table 3.3.2-1. The CCM relates as-designed module cost to IBP-MPCL program objectives and AEN metrics. The genesis of the IBP-MPCL baseline costs for the PNP and RF/FEC modules are itemized in Tables 3.3.2-2 and 3.3.2-3 respectively. The IBP-MPCL CCM estimate for the PNP is $18.6K and for the RF/FEC is $11.0K. In both distributions, custom ICs drive the total recurring cost of the design.

Table 3.3.2-1 IBP-MPCL vs. Military Cost Metrics

Attribute	Military Design to Cost	IBP-MPCL Commercial Cost Model
Production Time Span	15 Year	1 Year
Production Rate	Various by Year	200 PNP/100 FEC per Year
Inflation Adjustment	Various by Year	N/A (Current Year)
Material Technology Curve Application	Yes	N/A
Combined Procurement	442 Shipsets	15 Shipsets

Table 3.3.2-2 PNP DTC Current Summary

Cost Element	Military Baseline	IBP-MPCL	Percent Reduction
Touch Labor	2869	---	
Test Labor	1115	---	
Support Labor	3509	---	
Labor Total	7494	7062	**5.8%**
Standard Active Devices	2271	616	73%
Passive Devices	403	24	94%
Metal Fab /Hardware	3810	2144	44%
Custom Active Devices	21,982	8783	60%
Material Total	28,968	11569	**60%**
Total Module Cost	$35,962	$18,632	**48%**

Table 3.3.2-3 RF/FEC DTC Current Summary

Cost Element	Military Baseline	IBP-MPCL	Percent Reduction
Touch Labor	5495	---	
Test Labor	1119	---	
Support Labor	6125	---	
Labor Total	12,739	5246	**59%**
Standard Active Devices	3009	1121	63%
Passive Devices	527	53	90%
Metal Fab /Hardware	4015	2354	41%
Custom Active Devices	14,518	2313	84%
Material Total	22,069	5842	**74%**
Total Module Cost	$34,808	$11,088	**68%**

3.4 Technology Assessment and Application

Design and manufacturing technology assessments were made to avail the IBP-MPCL any advantage possible to improve compatibility with AEN and minimize cost of materials, parts, and processes, while maintaining or improving integrity. Technologies selected for evaluation were proposed on the basis to their relative applicability in accordance with the following criteria:

- Opportunity to reduce cost through simplification or process improvements

- Compatibility with potential new EPA regulations
- Opportunity to reduce module part count
- Compatibility with material lifetime cycles
- Compatibility with current and planned TRW AEN processes
- Opportunity to improve reliability
- Significant weight or size (real estate) advantages

A summary Technology Evaluation Matrix table was prepared in order to sort considered technologies into categories of materials, parts, and processes. Subsequently, each technology item in these categories was priority ranked. The purpose of the priority rank is to scope engineering effort in accordance with expected benefit of incorporation.

An assessment and evaluation was made of the applicability of new and emerging technologies considered for application on IBP-MPCL. For the purpose of the IBP-MPCL program, new and emerging technologies were defined as those not currently incorporated into the military design, or processes not currently established in the AEN factory. A detailed report of the evaluation of emerging technologies is presented in Table 3.4-1.

Table 3.4-1 Technology Assessment

Technology	Rationale	Attributes	Status
Lead Free Solders	Possible EPA Lead restrictions (5+ years). Passive evaluation at AEN	Expected few process mods, minimal cost impact (cost avoidance), "drop in" replacement available, durability characteristics unavailable	Outside program scope/duration
Adhesive Solder Replacement	Possible EPA Lead restrictions (5+ years). Passive evaluation at AEN	Conductive epoxy used for part attach	Not incorporated
Integral board core combination	Obviates board to core lamination process	Established technology, prototype experience at AEN , Large CTE mismatch, PTH reliability in question	Not incorporated
Multi-dielectric PCB	RF/FEC high speed clock circuitry requires isolation, eliminate SMAs and Coax	Eliminates semi-rigid cable and off-line assy. Wash out of cost impact, proven technology.	Not needed, requirement eliminated by design.
Ball Grid Array Packages	Improved manufacturability, High Assembly yields, cost and weight advantage	Coarse lead pitch, minimal component handling problems, SMT compatible, Limited temp. range	Incorporate PBGAs
Chip-on-Board/Flip-Chip	AEN has COB line experience. Opportunity for improved manufacturability.	Unpackaged devices are lower cost, denser packaging, fewer interconnects. Complex /expensive substrate required	Not incorporated.
Mixed mode ASIC, Consolidated IC	Potential component cost reduction, Higher manufacturing yield	Less dense boards, lower part counts, limited availability, significant-simulation	Very high NRE, cost benefit not likely in current IAR configuration.
Plastic Encapsulated Microcircuits	Cost savings (30-90%), Superior durability, improved compatibility with automation. Automotive industry standard.	Extended parts availability, reduced weight, higher moisture susceptibility, vendor quality varies. Reliability data available.	Fully incorporated
High Performance Conformal Coatings	PEM devices may need increased moisture resistance	Peck's model used to predict failure rate, conformal coat is additional barrier.	Silicone conformal coat utilized.
MCM-L Packaging	Substantial cost benefit over LTCC MCM	Larger Supplier base, weight savings, minimal integrity data available	MCM eliminated by use of discrete PBGA packages
Precision Solder Pads	Solder build-up of stand-off is desired, ASD multiple pass solder screen/reflow is expensive, cost reduction	Established process at board vendor, eliminates labor intensive screen process.	Not incorporated, AEN process for screen past is adequate.
Laser/Focused-Beam Soldering	Existing equipment at AEN, eliminates or reduces need for Hot Bar	Precision/tailored reflow schedule, high throughput, special fixturing required	Hot bar soldering incorporated.
Interconnect Crossover Alternatives	Crossover incompatible with AEN line, Off-line, process, flex expansion mitigation requires expensive material	Leadframe approach allows single sided installation, requires marginal additional area, compatible with laser soldering.	Did not incorporate, significantly less expensive flex crossover used.

3.5 Design Approach

3.5.1 Design Organization

Design for commercial manufacture, impacts the organizational structure, the engineering environment, the manufacturing environment, and the various systems that are in place. The Industrial Base Pilot (IBP-MPCL) explores each of these and developed the systems, policies, and practices required to have a design facility concurrently engineer a product with a remote manufacturing facility.

The successful manufacture of modules for the military aircraft is directly correlated to the ability of the PT IPT to manage, manufacture, design, and develop products from remote locations.

3.5.1.1 Structure of Organization

The adoption of a Triad Organizational Structure provides the links required to manage the project in multiple locations. The adoption of a Concurrent Product and Process Development (CPPD) structure bridges the distance between the design and manufacturing developments.

The triad organizational structure (Figure 3.5.1.1-1) is one where there is a responsible party at each of the three satellite organizations. The Project Manager (PM) has ultimate responsibility for making sure that the project is launched on time. The Responsible Manufacturing Engineer (RME) makes sure that the manufacturing process, systems, material, equipment, and labor are in place to produce the product. The Responsible Engineering Manager (REM) manages all of the design activities and personnel at all sites (commercial and military). This structure supports a cross functional, multiple location, concurrent engineering effort.

Triad Organizational Structure

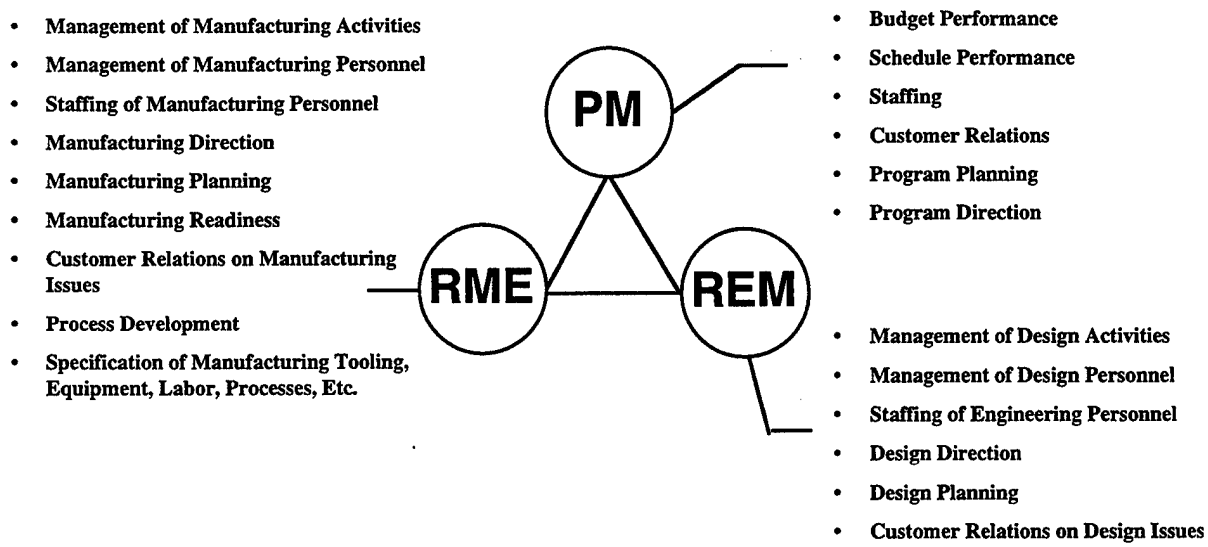

Figure 3.5.1.1-1 Triad Organizational Structure

3.5.1.2 Concurrent Product and Process Development (CPPD)

The CPPD process is being used for the IBP-MPCL for several reasons. Concurrent design and process development has been proven to reduce Engineering and Manufacturing Development (EMD) cycle time. Secondly, CPPD minimizes the number of redesigns that must occur as a result of incompatibility to the manufacturing processes. Thirdly, the CPPD process supports a system of satellite manufacturing and design development locations.

The particular CPPD process that has been adopted for the IBP-MPCL program is based on and tracked using a 33 Milestone Schedule. The 33 Milestone Schedule (Table 3.5.1.2-1) identifies key steps and reviews that impact the critical path. Each milestone has its own checklist that was used by the team to track what tasks have occurred in the completion of that milestone. For the IBP-MPCL program some of the milestones have been eliminated to fit the needs of the program, while others have been changed to take advantage of the military's approach to product validation.

Table 3.5.1.2-1 Concurrent Product and Process Development Process

#	Original 33 Milestones	IBP-MPCL 33 Milestones	Reason for Change
1	Awarded Business	Awarded Business	
2	Team Kickoff Meeting	Team Kickoff Meeting	
3	Program Plan Review	Program Plan Review	
4	Specification Review	Specification Review	
5	Program Concept Review	Program Concept Review	
6	**Test Plan Approval**	**Plan Development**	**Phase II Tasks Start Here**
7	Analytical Design Review	Analytical Design Review	
8	**Order E.V. Parts**	**Order DOE Parts**	**Military Validate Design**
9	**Engineering Validation Build - E.V.**	**Simulation: Module**	**Based on Simulation**
10	**1st Sample Submission**	**Simulation: Rack**	**Data Due to Low Volumes**
11	Component Supplier Build	Component Supplier Build	
12	Preliminary Design Review	Preliminary Design Review	
13	Preliminary Program Review	Preliminary Program Review	
14	Prototype Tooling	Prototype Tooling	
15	Procure Long Lead Items	Procure Long Lead Items	
16	Design Validation Build -D.V.	D.V. Build	
17	**2nd Sample Submission**	**1st Sample Submission**	**1st Samples Built at D.V.**
18	D.V. Testing	D.V. Testing	
19	Critical Design Review	Critical Design Review	
20	Critical Program Review	Critical Program Review	
21	Engineering Release	Engineering Release	
22	Engineering Release Sign off	Engineering Release Sign off	
23	Manufacturing Readiness	Manufacturing Readiness	
24	Customer Launch Readiness	Customer Launch Readiness	
25	Product Validation Build - (P.V.)	P.V. Build	
26	P.V. Testing	P.V. Testing	
27	P.V. (ISIR/ISW/GP3) Approval	P.V. (ISIR/ISW/GP3) Approval	
28	Obtain Production Material	Obtain Production Material	
29	Launch Readiness Review	Launch Readiness Review	
30	Obtain Customer Approval	Obtain Customer Approval	
31	Supplier Job #1	Supplier Job #1	
32	Customer Job #1	Customer Job #1	
33	Change Requests for Improvements	Change Requests	

3.5.2 The Design Environment

IBP-MPCL modules are derivatives of military designs. Modules must be capable of reliably functioning as demanded by deployed platform missions. This means that the IBP-MPCL modules must physically and electrically interface to existing systems, and continue to operate within the boundaries of the environment imposed by the air vehicle operating profile. In order to ensure this operability, yet allow unconstrained design options to optimize compatibility with industrial parts, materials, and processes, pilot module attributes were defined and identified as fixed or variable.

Fixed Attributes

Fixed attributes were derived from the military design baseline. These attributes define physical, electrical, and thermal features such as the interface connector, power supply and thermal load. Table 3.5.2-1 lists key requirements that drive the design of the IBP-MPCL modules.

Table 3.5.2-1 Key IBP-MPCL Design Drivers

Parameter	Requirement / Goal	Military Baseline
- Weight (#)	1.30 max	1.40
Durability/Integrity		
Damage Index - LCF	20 yr. life	0.42 TDI
Damage Index - HCF	12800 hrs.	0.01 VDI
Cumulative Damage Index	0.50 max.	0.43 CDI
Rack Interface	Pin/Part Compatible with military	Complies
EMI/EMC	Comply with Spec	Complies
Power	≤ Military	Complies
Thermal Management - Tj °C	105 max.	107
Size / Envelope (inches, max)		
Thickness	0.58"	0.58"
Width	5.960"	5.75"
Length	6.703"	6.69"
Electrical Performance	Comply with all Specs / requirements	Complies

Variable Attributes

Variable attributes are those design features that may by changed from the military baseline without necessarily violating physical and electrical operational integrity. These attributes are addressed during design evaluation and trades by concurrent engineering of module parameters such as board and core materials and component parts, as well as design accommodation of commercial manufacturing process flows.

Several key design-induced attributes have been determined to afford the most opportunity for achieving low-cost industrial manufacture. These are:

- Component Parts
- Board Materials
- Core Materials
- Solder Joint Process
- Active Component Package Materials
- Process Flow Sequence
- Electrical Component Screening

3.5.3 Design Approach

The design was performed with the other IBP-MPCL Integrated Product Teams (BP and MI), as well as with the commercial manufacturing partner TRW AEN.

Tasks were identified for the establishment of IBP-MPCL module conceptual designs. Key conceptual design tasks are as follows:

- Identify and categorize design attributes into fixed and variable design parameters.
- Determine which variable parameters have largest opportunities for redesign.
- Develop a design approach and scoring system that addresses these opportunities.
- Create and evaluate (score) conceptual designs.
- Perform experimentation and validation.
- Analyze and qualify enabling technologies.
- Select concurrent engineering environment tools to unite with commercial partner.

3.5.4 Part Driven Design

The most significant effort of the design process was to determine an appropriate selection of parts, given their performance with respect to the technical goals and interaction effects. The design trial selection process involved considerable iteration of part group postulation, with subsequent performance simulation, experimentation, analysis, and evaluation. Evaluation resulted in a relative figure of merit that was used to rank various design concepts. Figure 3.5.4-1 outlines the IBP-MPCL parts driven design approach.

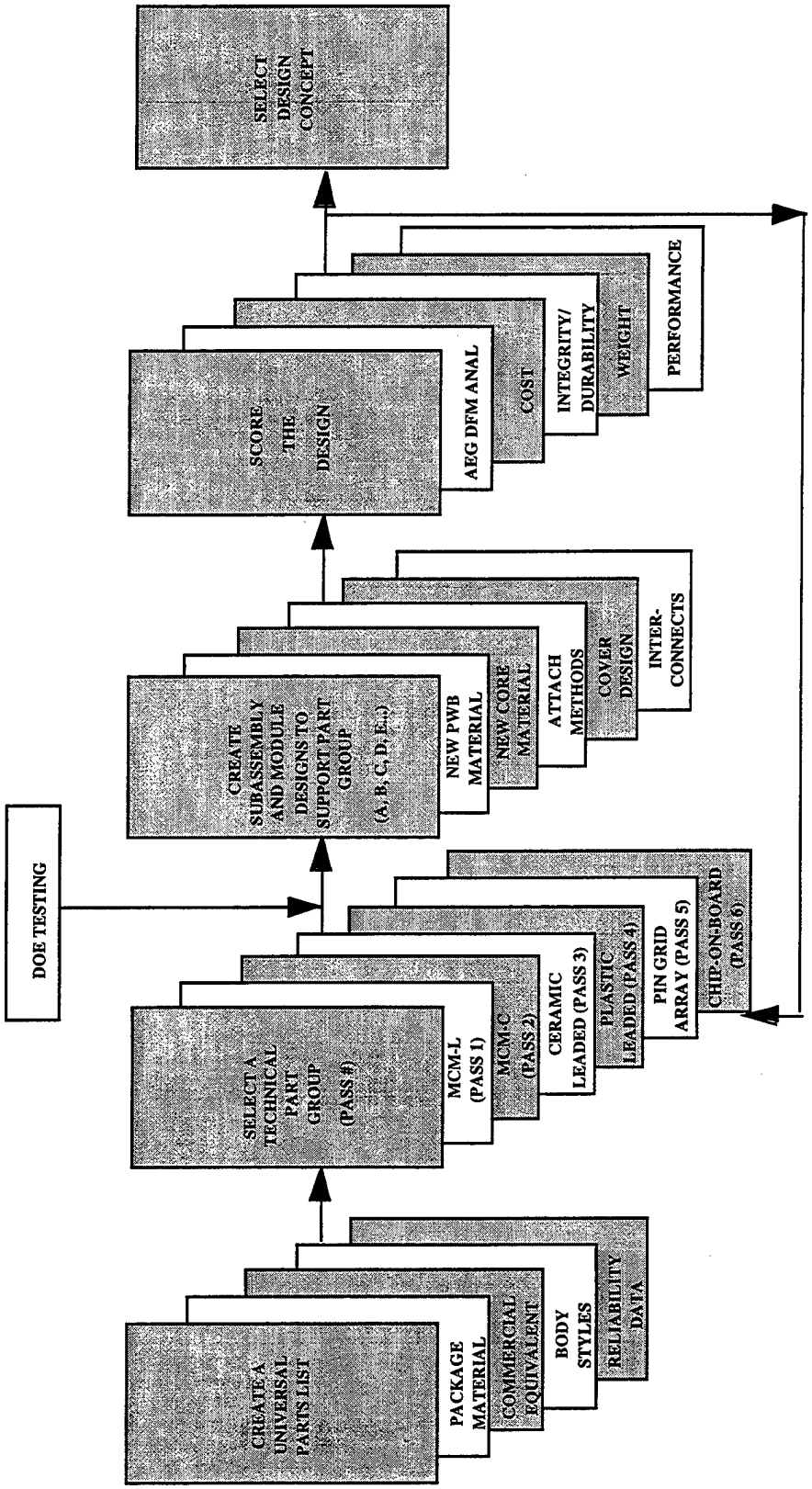

Figure 3.5.4-1 IBP-MPCL Parts Driven Design Approach

3.5.5 Design Scoring

One of the products that resulted from work done in Phase I was the Design Evaluation Matrix. The Design Evaluation Matrix (DEM) was developed by the PT IPT as a tool to use in the selection of a commercially manufactured military design. The DEM evaluates each of these packaging options based upon algorithms that were developed by the PT IPT. Elements of the DEM include the following:

- Durability Life
- AEN DFM Score
- Transferable Methodology
- Recurring Cost
- Life Cycle Cost
- Weight
- Commonalty to Alternate Platforms
- Technical Risk of Design Approach
- Non-Recurring Expense (NRE) to Industrial Base Pilot (IBP-MPCL)
- Fit to the military Rack
- Functionality

An algorithm was developed for each element in order to score the various designs. The results of the scoring determined which design was developed and manufactured for the Design Validation Build in Phase II of the IBP-MPCL program. Scoring of selected design passes is presented in Section 3.6.7.

3.6 Conceptual Design

Conceptual designs were created and various design passes were selected and evaluated to include as many different part/package types as practical. For each pass, the part type mix was chosen to limit "mixed technology", improving the manufacturability of the final design. There were 29 independent design passes utilizing combinations of core material, printed circuit board (PCB) material, attach method, cover design, and interconnect scheme with the six ASIC and MCM package styles. From the 29 independent designs, six principle conceptual designs were selected, which are identified as follows:

Pass 1: Plastic Ball Grid Array

Pass 2: Ceramic Ball Grid Array

Pass 3: Ceramic Leaded

Pass 4: Plastic Leaded

Pass 5: Pin Grid Array

Pass 6: Chip on Board

Table 3.6-1 shows a matrix of part types chosen for each design pass.

Table 3.6-1 Conceptual Design Pass Matrix

	Part Types		
Pass	**DSP MCM**	**ASICs**	**I.C.s**
Baseline	Ceramic QFP	Ceramic QFP	Ceramic QFP, FP and LCCs
1	MCM-L PBGA	PBGA	Plastic SOPs, FP, QFP & PBGAs
2	Ceramic BGA	Ceramic BGA	Mix-Plastic/Ceramic SOPs, FP & QFPs
3	Ceramic Leaded QFP	Ceramic Leaded QFP	Mix-Plastic/Ceramic SOPs, FP & QFPs
4	Plastic Leaded QFP	Plastic Leaded QFP	Mix-Plastic/Ceramic SOPs, FP & QFPs
5	Pin Grid Array	Pin Grid Array	Mix-Plastic/Ceramic SOPs, FP & QFPs
6	Chip-on-Board	Chip-on-Board	Chip-on-Board

For the military baseline, design constraints for part types included commonality within the military CNI designs (i.e., DSP MCM), Military approved parts availability, board real estate and assembled component height. The military baseline design for the PNP and the RF/FEC materials consists of polyimide glass boards hard bonded to silicon-carbide aluminum cores.

With the part mix for each IBP-MPCL design pass established, the next procedure was to define materials that would support each design. A goal of each design pass was to select a range of compatible thermal cores, PWB and core bond adhesives for evaluation. Thermal core materials considered included 6061 Aluminum, Beryllium/Beryllium Oxide (BeBeO), P120 graphite/epoxy and K1100 graphite/epoxy. Silicon-carbide aluminum (SiCAl) cores were not specifically evaluated since considerable data was available from the military program. Further, the SiCAl core exhibits properties similar to the BeBeO core. PWB materials considered included BT or Tetra-Functional Epoxy Glass, Polyimide glass, Epoxy Aramid (non-woven) and LTCC Ceramic. Board to core attachment was soft bond (mechanically compliant bond), hard bond, or screw fastened assembly. These materials were selected primarily to establish a range for thermal characteristics, weight, stiffness and coefficient of thermal expansion. Each design was evaluated against all of the Design Scoring elements described in Section 3.5.5.

LRM configurations chosen for design passes provide a range of mechanical characteristics for durability and thermal performance trade studies. Key components are the thermal conduction core, PWB material, and the PWB to core mechanical connection. For purposes of trade studies, other components were assumed to be the same as the military baseline, e.g. covers, connectors, crossovers, and wedgelocks. Core thickness of 0.050" was used throughout. From military experience, it is known that core materials would require key mechanical properties as good as Aluminum (Modulus, 10 Msi; thermal conductivity, 3.9 W/in/°C). For example, copper (good thermal conductivity) was not considered because it's specific stiffness and specific conductivity are both worse than aluminum. Other core materials considered for this application include graphite composites (P120 and K1100) which exhibit thermal conductivities in the range of 6-10 W/in/°C, and a metal matrix composite (BeBeO) which exhibits thermal conductivity of 9 W/in/°C. All the composite materials have specific properties superior to aluminum.

CTE matching for plastic components is best accomplished using a compliant adhesive (Silicone based, for example). Compliant bonds decouple strains from core to PWB. In this type of construction, the PWB material, that is a better match to plastic components, controls CTE. CTE match for ceramic components is accomplished using hard adhesives (epoxy based, for example). Hard bonds couple the PWB to the core. In this type of construction, the core material that is optimal for durability controls CTE when it matches ceramic (4-7 ppm/°C). In these applications metal matrix composites are superior.

3.6.1 Pass 1 Plastic Ball Grid Array (PBGA)

This design was intended to take advantage of commercial plastic ball grid array (PBGA) packages. These plastic parts offer a 24% reduction in part weight compared to the baseline military parts. Further weight reduction is realized by using core, board and cover materials that are lighter than the military baseline. One of the concerns with the PBGAs is the thermal characteristic of the plastic. Much of this concern is offset because of the excellent thermal path between the package substrate and board. For high cycle fatigue (vibration), material combinations must be chosen which provide a sufficiently stiff platform with low amplification factors (Q) to limit board deflection. For low cycle fatigue (thermal cycling), the material combination must be chosen to closely match the CTE of the plastic components (approx. 17 ppm/°C) to avoid premature failure in the solder. Published studies have demonstrated that die attachment also significantly affects the local CTE; therefore, material combinations must also avoid significant CTE mismatch within local areas under the die (approx. 9.8 ppm/°C).

The risks associated with Pass 1 are the following electrical and mechanical issues. Mechanical risks include:

a) heat removal from the package

b) plastic package moisture absorption

c) solder ball uniformity

d) solder ball joint integrity

e) reworkability

Electrical risks associated with PBGAs include:

a) ability to route signals through the substrate in order to establish predictable capacitance and inductance between pins

b) ability to probe the package,

c) calculation of timing based on anticipated package characteristics (performance should be better than the current leaded devices),

d) Re-creation of test vectors based on new pin outs

e) re-analysis of board design routing.

3.6.2 Pass 2 Ceramic Ball Grid Array (CBGA)

This design concept was intended to take advantage of ball grid array (BGA) package technology but avoid the risk of introducing plastic parts to the design. This parts mix

offers a 5% reduction in parts weight compared to the Baseline military parts. Further weight reduction is realized by using core, board, and cover materials that are lighter than the military baseline. As with the plastic ball grid array package, this option provides an excellent thermal path between the package case and board. For high cycle fatigue, material combinations must be chosen which provide a sufficiently stiff platform with low amplification factors (Q) in order to limit board deflection. For low cycle fatigue material, combinations must be chosen to closely match the CTE of the ceramic (approx. 6.5 ppm/°C) to avoid premature failure in the solder.

The risks associated with Pass 2 are the following electrical and mechanical issues. Mechanical risks consist of

a) solder ball uniformity

b) solder joint integrity

c) reworkability

Electrical risks associated with CBGAs are

a) ability to route signals through the substrate in order to establish predictable capacitance and inductance between pins

b) ability to probe the package

c) calculation of timing based on anticipated package characteristics (performance should be about as good as the current devices). CBGAs exhibit lower lead inductance than PBGAs; however, CBGAs have a higher dielectric, about 9.5, as compared with PBGAs,

d) re-creation of test vectors based on new pin outs, and e) re-analysis of board design routing.

3.6.3 Pass 3 Ceramic Leaded

This pass was considered the lowest risk packaging approach. This parts mix results in a 1% increase in parts weight compared to the baseline military design; however, weight reduction is realized by using core, board, and cover materials which are lighter than the military baseline. Thermal characteristics of this part mix are comparable to the military baseline. For high cycle fatigue, material combinations are chosen to provide a stiff platform with low amplification factors (Q) to limit board deflections. The use of adhesives between the part and the board could provide highly durable solder joints and leads while minimizing the need for exotic materials to stiffen the cores. For low cycle fatigue, material combinations must be chosen to match the CTE of the ceramic (approx. 6.5 ppm/°C) to avoid premature failure in the solder. However,

because of compliance provided by device leads, there is more tolerance for a CTE mismatch.

The risks associated with Pass 3 are the following electrical and mechanical issues. Mechanical risks appear to be limited only to placement of fine pitch leaded devices. The electrical risk associated with ceramic leaded devices is that they exhibit larger inductance than some other packaging types. However, risk due to the use of ceramic parts is low because the current design is based on these types of devices.

3.6.4 Pass 4 Plastic Leaded

This pass was intended to be the commercial equivalent of the ceramic leaded approach. It provides the advantages of the ceramic leaded design pass, but introduces the risk associated with use of plastic parts in the military environments. This part mix results in a 21% decrease in parts weight compared to the baseline military parts mix. Further weight reduction is realized by using core, board, and cover materials that are lighter than the military baseline. Thermal performance of this design is the poorest of any of the options analyzed. In order to implement this option, it is necessary to use a core with extremely high thermal conductivity in order to keep junction temperatures down. For high cycle fatigue, material combinations must be chosen which provide a stiff platform with low amplification factors (Q) to limit board deflection. The use of adhesives between the part and the board could provide highly durable solder joints and leads, while limiting the need for stiffer cores. For low cycle fatigue, the material combinations must be chosen to match the CTE of the plastic (approx. 14 ppm/°C) to avoid premature failure in the solder. However, because of lead compliance, there is more tolerance for CTE mismatch. In addition, a CTE match near 17 (plastic) instead of 6.5 (ceramic) is achievable with a wider range of standard.

Risks associated with Pass 4 are the following electrical and mechanical issues. Mechanical risks consist of

a) placement of fine pitch leaded devices

b) moisture absorption into plastic packages

c) removing heat from plastic packages

d) availability of all devices in plastic leaded packages.

Electrical risks associated with plastic leaded devices are

a) high lead inductance (this could cause timing problems and larger crosstalk),

b) re-creation of test vectors based on new pin outs

c) re-analysis of board design routing.

3.6.5 Pass 5 Pin Grid Array (PGA)

This design pass was intended to provide a highly durable component attachment with limited board real estate. This parts mix results in a 43% increase in parts weight compared to the baseline. Use of core, board, and cover materials that are lighter than the baseline would make it difficult to realize weight reduction since the predominance of the weight is due to the parts. In addition, this part mix failed the go/no-go scoring parameter of fit due to assembled component height. Therefore, little effort was expended on further analysis.

The risks associated with Pass 5 are the following electrical and mechanical issues. Mechanical risk is primarily due to lack of availability of component devices in pin grid array packages. The electrical risks associated with PGA devices include a) high lead inductance (this could cause timing problems and larger crosstalk) b) re-creation of test vectors based on new pin outs, and c)re-analysis of board design routing.

3.6.6 Pass 6 Chip on Board (COB)

This design pass was considered because it potentially could provide the lowest weight, best durability, and the best thermal characteristics. The elimination of the component packages results in a 94% reduction in "parts" weight compared to the military baseline. Further weight reduction is realized by using core, board and cover materials that are lighter than the military baseline. Thermal characteristics of this pass are excellent for a wide range of core/board materials. There was no durability model (high or low cycle) developed for this pass. This design is expected to be highly durable because of the lack of interconnect solder joints, which are the largest durability risk.

Risks associated with Pass 6 are the following electrical and mechanical issues. Mechanical risks include

a) The assembly line at AEN is not currently capable of this product type

b) uncertain availability of known good die (reworkability risk).

Electrical risks associated with COB include

a) potential circuit timing hold problems due to interconnect inductance differences from the military design

b) re-creation of test vectors based on new test philosophy and added test points for visibility

c) re-analysis of board design routing.

3.6.7 Conceptual Design Scoring

The PT Team developed a quantitative scoring matrix. The matrix prioritizes the importance of potentially competing attributes of the design and is noted in Section 3.7.9. Within each category of the matrix, critical drivers were determined and segregated to assist in scoring a design concept equitably in all areas. These parameters are illustrated in Table 3.6.7-1.

Table 3.6.7-1 Design Scoring Parameters

Scoring Parameter	Drivers	Wt
Durability/Life	CTE Mismatch, Natural Frequency, Thermal characteristics used to evaluate high and low cycle fatigue using tuned spreadsheet analysis.	10
AEN DFM Score	Design for Assembly Software Score, Quality Model Output, Factory Simulation Results, Manufacturing Cost Model Data, and Quality Model predictions	10
Transferable Methods	Domestic Commercial Manufacturing Resources that could produce this product	8
Recurring Cost	BOM and Labor Cost	8
Life Cycle Cost	Reliability, Serviceability and Logistics impact	7
Weight	Bill-of-materials for each design pass used to determine estimated weight.	6
Commonalty	Junction Temperatures used to determine capability of design to meet reliability requirements on other platforms.	4
Technical Risk	Predicted impact on electrical performance, uncertainty in mechanical performance data, commonalty with AEN production capability.	4
Non-Recurring Expense	Design Cost, Tooling and new Capital Equipment	8
Fit to the military Rack	Go/No-Go parameter based on board real estate and assembled component height.	G/N
Functionality	Go/No-Go parameter based on ability of new design to duplicate functionality of military design	G/N

A detailed algorithm to quantify the analytical results of a design pass was developed for each parameter. The algorithm for Durability is shown in Figure 3.6.7-1.

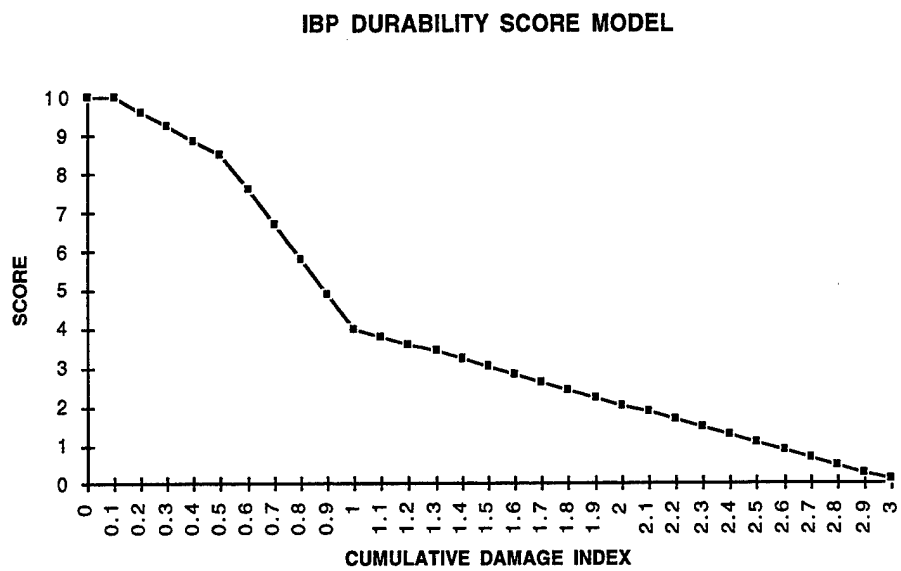

Figure 3.6.7-1 Durability Scoring Algorithm

For each design pass, Low and High cycle (thermal cycle and vibration) damage indices were calculated and summed to create the Cumulative Damage Index (CDI). The quantitative score was determined by moving along the Y-axis to find the intercept with the CDI. The shape of the curve places a severe penalty on designs exceeding a CDI of 1.0, theoretical 1 life, and provides diminishing benefit for designs that exceed a CDI of 0.5, or better than two lives. This encourages designs to meet or exceed a theoretical life, but does not artificially incentivize optimization for exceptional life, as this has little marginal value. The theoretical values may contain large errors due to uncertainty in modeling commercial materials and components used in these designs.

Figure 3.6.7-2 shows the algorithm for Recurring Cost.

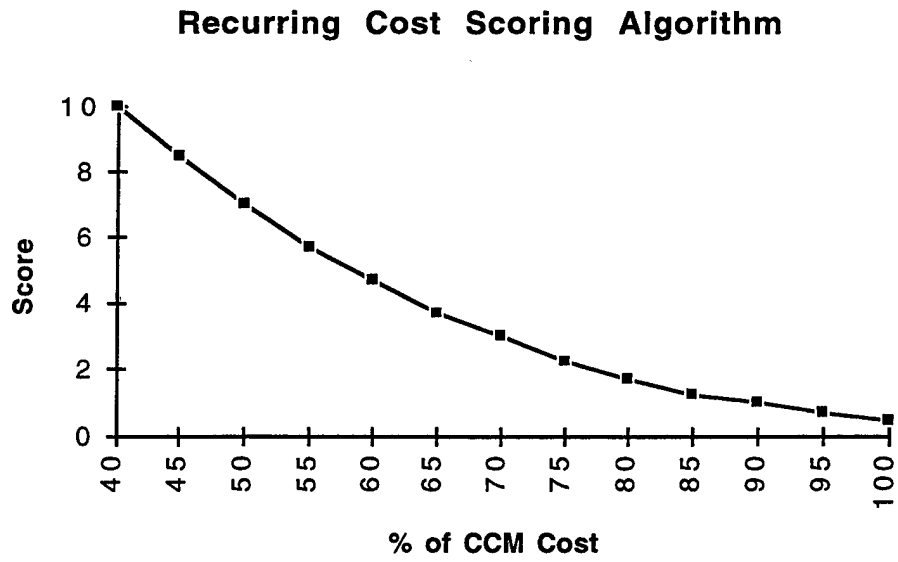

Figure 3.6.7-2 Recurring Cost Algorithm

The total Bill of Material (BOM) and labor cost were calculated for each design pass and ratioed as a percentage of the military costs applied to the Commercial Cost Model (CCM). The quantitative score was determined by moving along the Y-axis to find the intercept with the percentage of the CCM cost. The shape of the curve places an emphasis on meeting or exceeding the pilot program objectives of 50% reduction in cost. Figure 3.6.7-3 gives the relationship for Life Cycle Cost.

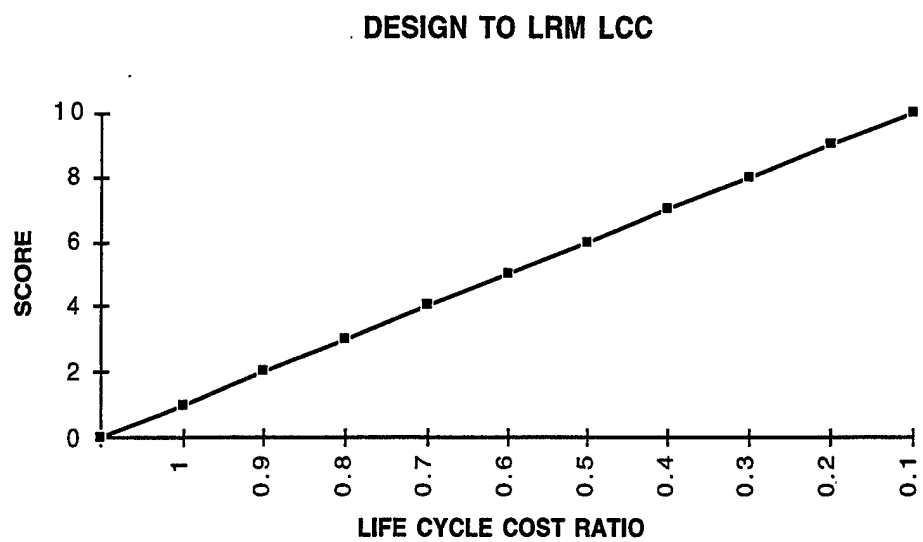

Figure 3.6.7-3 Life Cycle Cost

Life Cycle Cost (LCC) is calculated by evaluating life cycle variables: Repairability, Maintainability, Testability, Reliability, and Durability. Such factors as part obsolescence, test and repair equipment, device operating temperature (device reliability) are included. The LCC ratio is the total of these factors divided by the military baseline. The score is determined by moving along the Y-axis to find the intercept with the ratio. This relationship is linear as lower ratios indicate continuing increases in performance.

Commonalty Algorithm is shown in Figure 3.6.7-4.

Limiting peak junction temperatures such that they remain within reliability limits for military as well as other platforms fosters commonality. All other platforms considered have more severe thermal environments than the baseline. Commonality with current military designs is difficult to achieve with PBGAs, as well as with all plastic packages, due to poor thermal spreading in the plastic substrate under the die. Thermal analysis indicates that peak junction temperatures exceed 125°C for all LRM configurations analyzed. High temperatures occur for relativity few components and may be reduced with local temperature reduction techniques.

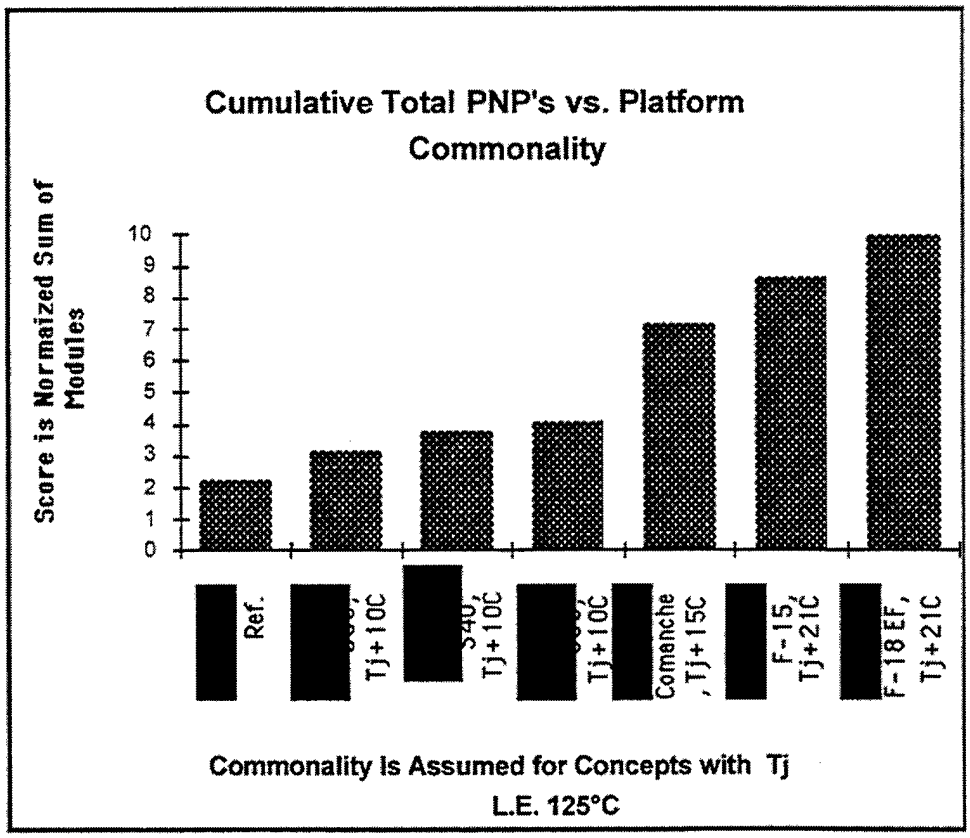

Figure 3.6.7-4 Commonalty

Commonalty of designs is determined by device junction temperature, T_j. Life on platforms other than the baseline are constrained by higher operating temperature, which relates to less reliable, shorter lived electronic parts. To score designs for commonalty, the design's worse case junction temperature was calculated, the platforms increased operational temperature was added, and evaluated against a "worse case "reliability of operation at 125°C. If a design's electronics stayed below 125°C, it was scored successful. As can be seen in Figure 3.6.7-4, platforms are arranged in order of increasing operating temperatures. The Commonalty score is determined by moving along the Y-axis to find the intercept with the total platforms served by the design. This relationship increases with platforms at a rate determined by the quantity of modules that are used by that platform.

The algorithm for weight is shown in Figure 3.6.7-5.

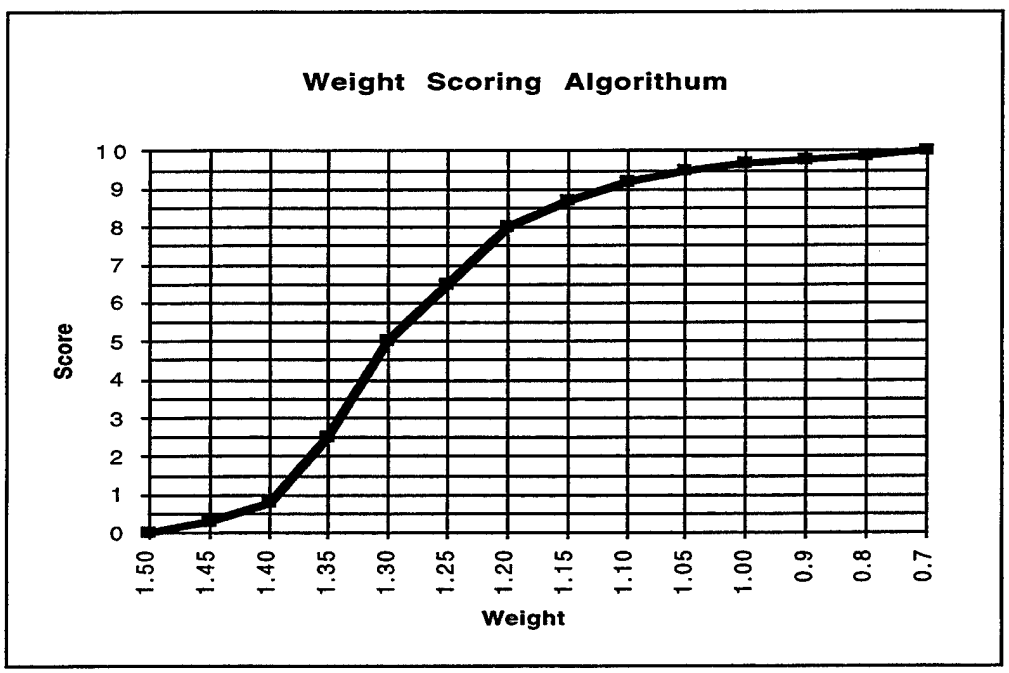

Figure 3.6.7-5 Weight Algorithm

Once the theoretical weight of a design was calculated, the quantitative score was determined by moving along the Y-axis to find the intercept with the weight. The shape of the curve places a severe penalty on designs exceeding the target weight of 1.30 lb and provides diminishing benefit for weights below 1.1 lb. This encourages designs to meet or exceed the baseline, but does not artificially incentivize optimization for weight savings.

The scoring methodology for Design for Manufacturability is shown in Figure 3.6.7-6. This matrix provides the algorithm for determining the DFM score for a design based upon the manufacturability of candidate designs using specific producibility measures established at the AEN facility. It can be seen from this table that important manufacturability factors include consideration of number of non-standard processes, conformance to design guidelines, machine cycle time and set up time, etc.

After all the scoring algorithms were established, they were applied to each of the conceptual designs to determine a cumulative score. The results of this scoring is provided in Section 3.7.9.

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DESIGN for MANUFACTURABILITY SCORING MODEL

	Conformance to Current & Future TED ProcessesA		Conformance to Design GuidelinesB		Factory Simulation (WITNESS)C		Design for Assembly (DFA)D		MPCME		Quality ModelF		TOTAL	SCORE
Weight	10		5		8		5		8		10			
	Score	Total	Score	Total	Score	Total	Score	Total	Score	Total	Score	Total		
Baseline														
IBP Pass 1 - PBGA														
IBP Pass 2 - CBGA														
IBP Pass 3 - PQFP														
IBP Pass 4 - CQFP														
IBP Pass 5 - PGA														
IBP Pass 6 - COB														

Figure 3.6.7-6 Design for Manufacturability

3.7 Process Technology Phase I Summary

This section presents the results of the analyses that were performed in support of each of the design scoring algorithms and the selection of the "best" conceptual design for in the hardware builds performed in Phase 2 of the program.

As a result of the work performed in Phase 1, the packaging approach utilizing Plastic Ball Grid Array (PBGA) packages for the custom components and a mix of plastic and ceramic leaded components for the remaining active components was selected. TRW AEN Production Line #3 was selected for production of this design approach. Line #3 is a low volume high mix production line.

To perform this selection, each concept was evaluated over the factors listed in Section 3.6.7. A summary of the results is presented here.

3.7.1 Non-Recurring Costs

Each design concept was evaluated for its non-recurring cost to implement in three areas: Capital Equipment, Design Cost and Production tooling. Capital Equipment is the new production, assembly and test equipment required to produce the specific design approach on any of the AEN manufacturing lines in the Marshall facility. Design Costs are those one-time expenses associated with converting the existing military design to the proposed design concept. Production tooling costs are the one-time expenses of hard tooling the Marshall production line with product unique tools and the costs for suppliers of preparing to fabricate unique portions of the design. Capital equipment and tooling can be thought of as measures of negative incentives for the commercial company, because they are departures from their existing base.

The best performing concepts for NRE were those utilizing Ball Grid Arrays and Pin Grid Arrays. The Marshall automotive facility is ideally suited to adapt their conventional surface mount techniques to BGAs and has ongoing production in through hole technology. Therefore, the PGA and BGA have the lowest capital impacts, and lowest tooling impacts. BGAs have a moderate design impact. PGAs have a high design impact in re-engineering this densely populated surface mount design for through hole technology. Plastics are generally preferred over ceramics at Marshall due to a higher tolerance to automated tooling. The COB concept scored low in all three NRE categories; it has the highest capital equipment costs (Marshall has no chip and wire capability), the highest tooling costs, and would require the most exhaustive re-engineering of

the product. This effort is large due to the complicated redesign of the substrate and component availability in known good die.

3.7.2 Recurring Costs

Each design concept was evaluated for its recurring cost for the bill of material (BOM) and labor for assembly, test and support. The cost of the bill of material was developed by soliciting quotations and estimates from vendors using a basis of 100 PNP and FEC modules. To estimate the assembly and support labor figures, simulations were performed on each major design pass using the Witness simulation model. Witness Simulation is a software program that simulates line throughput, balancing, queuing, and yield. The simulated production scenario assumed 30 PNP and 30 FEC modules were independently introduced to the assembly line, with estimated product set-up times and process yields. The model results were used in the MPCM to calculate expected labor and support costs for each design approach. The labor and support rates used were standard for the Marshall facility, and did not include allowance for additional capital depreciation or fee (Profit).

The lowest recurring cost concepts were those utilizing chip on board and plastic BGAs or flatpacks. Chip on board cost estimates assumed full capitalization of chip and wire capability with depreciation amortized over military and commercial volumes. Plastic leaded packages and PBGAs offer the next best recurring cost approaches. Plastic devices are less expensive than the ceramic equivalent and they process well on the commercial manufacturing line.

3.7.3 Module Weight

Weights for the designs were derived from one of four sources: actual weights, scaling from similar known commodities, solid models, or engineering estimates. The lowest weight design approach is COB technology, due to elimination of the packages. The next lowest weight concepts were those utilizing plastic parts, both BGA and leaded.

3.7.4 Design Integrity (Durability Life)

A solid model was constructed for analysis of the design integrity of the various concepts, and critical parameters, such as fundamental frequency and module coefficient of thermal expansion were calculated. These parameters were then used in thermal and vibration analysis tools to calculate damage indices for each of the design concepts.

Designs with stiffer cores exhibited lower vibration damage indices. Designs with CTEs matched to the component and with component level stress relief exhibited lower thermal induced damages. Ceramic leaded devices on ceramic cores with hard attach of the PWB performed well in both categories. Likewise, plastic leaded devices on BT epoxy boards soft bonded to graphite cores performed well in both categories.

3.7.5 Design Commonality

Commonality scores were derived on the ability of the design to provide reliable performance for each prospective platform's mission. Designs that are reliable in multiple platforms scored best.

Alternate platform life requirements and environments, an assumption was made that vibration and thermal cycling effects would be roughly equivalent (or could be made to be equivalent in rack design) among platforms.

To address expected life on alternate platforms, the thermal derating of parts was addressed. Chip on Board concepts perform best due to their excellent θ_{JC}. These concepts were followed by ceramic packaged concepts, both leaded and BGA. Note that many plastic concepts have severe limitations for use in high temperature environments.

3.7.6 Design and Production Risk

This parameter qualitatively addresses the relative risk of the design approaches. Risk areas include electrical performance, mechanical integrity, manufacturability, prevalence of the technologies used in the market (both military and commercial), number of sole sources involved and the cost to recover from a failure.

Chip on board concepts were highest risk, while leaded ceramic packages are the least risky for these applications. Graphite cores present a higher risk than ceramic or Aluminum cores, and Aramid PWBs are higher risk than conventional glass systems.

3.7.7 Life Cycle Cost

Life Cycle Cost is calculated by evaluating life cycle variables: Repairability, Maintainability, Testability, Reliability, and Durability. Part cost, obsolescence, part operating temperature, ease of repair, and diagnostics are all considered.

All designs were considered equivalent for part obsolescence. The shorter life cycles for the plastic parts were balanced by the mass production and

distribution availability. The ceramic parts had longer life spans, but limited availability. Leaded design concepts were preferred for testability (ability to do probe level diagnostics), while COB designs were judged weakest due to full part encapsulation. Both styles of plastic parts, leaded and BGA scored best due to their lower procurement costs.

3.7.8 AEN DFM Analysis

The manufacturability in the commercial facility of each concept is considered here. AEN has several tools used to quantify manufacturability of a commercial design, MPCM, QM, PFMEA, DFMEA, and line simulation (Witness). The output of each of these DFM tools was combined to create a DFM score for each of the concepts based on the proposed combination of parts, boards, cores and hardware.

Concepts using fewer parts performed better. Plastic through hole and surface mount parts performed better than ceramic due to the facility tooling. BGA concepts evaluated better than fine pitch leaded concepts due to better Quality Model predictions (lower PPM) for BGA than fine pitch (0.020 and 0.015" lead centers). Mechanical fastened boards are preferred over bonded concepts.

3.7.9 Design Decision Matrix

After scoring each independent parameter, the combined scores were included in the decision matrix introduced in Section 3.5.5. The matrix (Table 3.7.9-1) includes each design pass on the left column and the factor "weight" (importance) on the top row. The numbers in the matrix are the result of the product of the concepts raw "score" in a category by the "weight".

Two parameters, Fit and Function, where considered binary; a concept either scored 0 or 1. 200 points were used to offset design concepts that would require mechanical redesign (0 for Fit) or software/interface changes (0 for Function). Italicized rows indicate pass champions or "best in class". The bolded row is the highest overall score, and represents the best quantitatively scored design.

The team also conducted qualitative scoring of the design passes and selected pass 1E for follow-up detailed design for Phase 2.

Table 3.7.9-1 Design Evaluation Matrix

DESIGN APPROACH	NRE DESIGN CAPITAL & TOOLING	RECURRING COST	WEIGHT OF MODULE	FIT	FUNCTIONALITY	DURABILITY	COMMONALITY TO PLATFORMS	TRANSFERABLE METHODOLOGY	TED DFM ANALYSIS	LIFE CYCLE COST	TECHNICAL RISK OF APPROACH	TOTALS
FACTOR "WEIGHT"	4	8	6	200	200	10	4	8	10	7	4	
Military DESIGN	16.4	4	21	200	200	89	18.4	0	38.9	7	36.4	629.1
PASS 1A	16.8	46	42	200	200	0	0	56	100	33.6	28.4	722.8
PASS 1B	16.8	39.6	52.5	200	200	34	0	56	90	49	24.8	762.7
PASS 1C	16.4	46	39	200	200	0	0	56	91	42.7	28.8	720.0
PASS 1D	16.8	39.6	54	200	200	76	0	56	90	51.8	24.8	809.0
PASS 1E	**16.4**	**39.6**	**54**	**200**	**200**	**85**	**0**	**56**	**90**	**51.8**	**24.4**	**817.2**
PASS 1F	16.4	41.2	52.56	200	200	0	0	56	96.7	29.4	27.6	719.9
PASS 1G	16,4	38	52.2	200	200	38	0	56	80	48.3	26	755.3
PASS 2A	*16.4*	*24*	*42*	*200*	*200*	*85*	*0*	*56*	*77.8*	*42*	*28.4*	*771.6*
PASS 2B	16.4	25.2	48.3	200	200	0	0	56	86.7	28.7	28	688.9
PASS 2C	16.4	19.2	42.6	200	200	85	0	56	74.4	38.5	28	760.1
PASS 2D	16.4	26.4	39.6	200	200	19	0	56	91.1	36.4	29.2	714.1
PASS 3A	12.8	38	27.6	200	200	0	0	56	61.1	51.8	36	683.3
PASS 3B	*12.8*	*33.2*	*45*	*200*	*200*	*94*	*0*	*56*	*53*	*49.7*	*32*	*778.6*
PASS 3C	12.8	36.4	31.2	200	200	0	0	56	47.8	30.1	34.8	649.1
PASS 3D	12.8	31.6	43.2	200	200	67	0	56	50	46.9	32	739.1
PASS 3E	12.8	31.6	39	200	200	100	0	56	44	49	32.4	765.2
PASS 4A	8.8	48	42	200	200	58	0	56	66.7	54.6	28.4	762.5
PASS 4B	8.4	42.8	52.5	200	200	100	0	56	55.6	54.6	24.4	794.3
PASS 4C	8.4	44.4	46.2	200	200	100	0	56	53.3	56	27.6	791.9
PASS 4D	*8.8*	*44.4*	*51.3*	*200*	*200*	*100*	*0*	*56*	*68.9*	*56*	*26*	*811.4*
PASS 4E	8.4	39.6	49.5	200	200	100	0	56	42.2	53.9	25.2	774.8
PASS 4F	8.8	42.8	48	200	200	100	0	56	60	54.6	25.2	795.4
PASS 5A	*3.2*	*50*	*2.4*	*0*	*200*	*50*	*0*	*80*	*58.9*	*57.4*	*24.4*	*526.3*
PASS 6A	0	56	56.4	200	200	89	9.2	32	36.7	59.5	22	760.8
PASS 6B	0	46	57.6	200	200	89	0	32	26.7	56	22	729.3
PASS 6C	*0*	*50.4*	*58.8*	*200*	*200*	*89*	*40*	*32*	*44.4*	*57.4*	*20.4*	*792.4*
PASS 6D	0	46	59.1	200	200	89	40	32	31.1	56	19.6	772.8
PASS 6E	0	44.4	58.62	200	200	89	40	32	23.3	54.6	20	761.9
PASS 6F	0	46	59.1	200	200	89	40	32	31.1	55.3	18.8	771.3

Italicized rows are Pass "Champions"
Bolded Row is Overall "Champion"

4.0 DESIGN

The hardware chosen to demonstrate the IBP-MPCL process had a baselined design. This baseline represented a military methodology and approach for design and manufacturing. The redesign effort required creation of a complete new design package from schematics to assembly drawings as well as testing and analysis to evaluate prospective changes. This section discusses the design process used and details the analysis and testing performed to characterize the design.

4.1 Design Documentation

4.1.1 Parts Selection

The primary methods and processes used for selecting the parts for the Industrial Base Pilot program were detailed as part of the Business Practices (BP) effort. The results of which were documented in the Business Practices Handbook.

The detailed criteria used for selecting the parts to support the hardware production are described in this section.

As part of the conceptual design process, the initial task was to create a parts list that addressed the needs of the specific avionics application as well as comply with the design for manufacturability criteria.

The key criteria that were focused on to meet these needs were as follows:

1) Industrial temperature rated components (-40C to +85C), or better, were to be used as much as possible.

2) Any existing (AEN) automotive parts that were available and met the design performance requirements would be used.

3) Surface-mount, commercially available, plastic microcircuits that met the following:

   a) electrical design functional requirements

   b) package outlines under .150" high

   c) package lead pitches 20mils, or greater

   d) same die technologies for devices used on original military design (whenever possible)

4) Use parts that have supporting qualification and reliability data from the suppliers.

5) Use parts that are validated through the IBP-MPCL component reliability (CR) testing and design of experiments (DOE) testing.

Eventually, a quantity of approximately 120 parts were selected to support the hardware production build for the 2 module designs. The category breakout for these parts is shown in Figure 4.1.1-1.

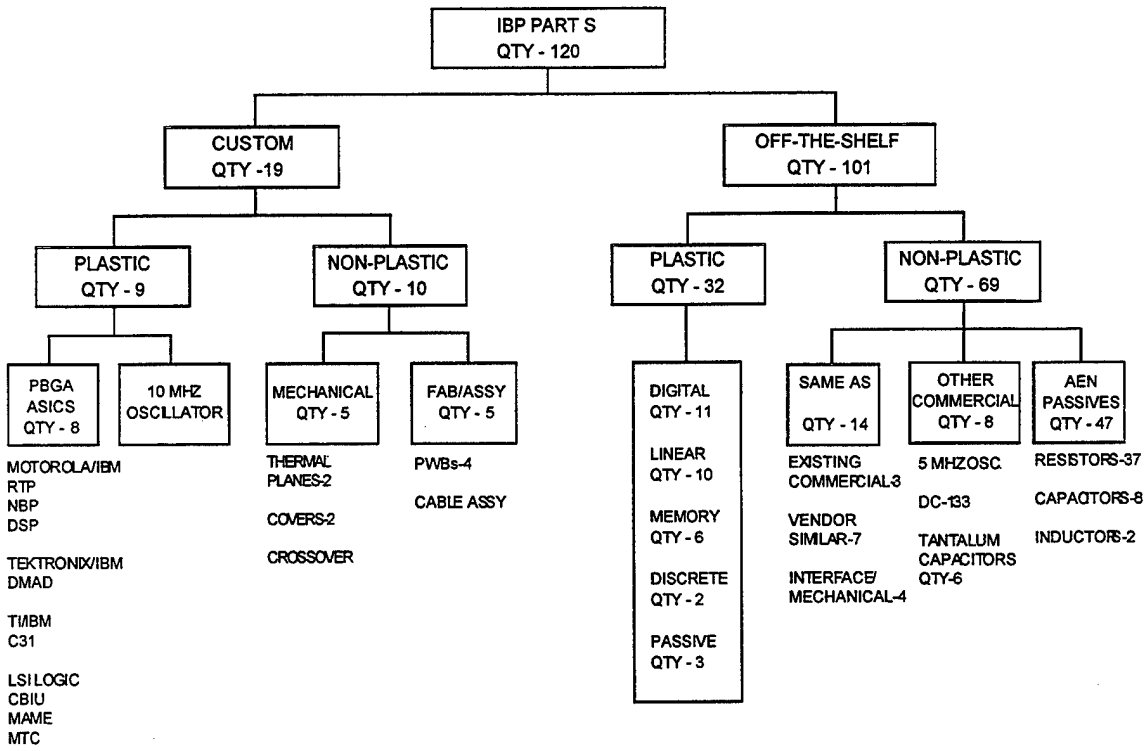


Figure 4.1.1-1 Categories of Selected Parts for the IBP PT module builds

Adoption of commercial / industrial microcircuits and passive components, had a number of advantages for this design. Use of commercial components take advantage of the increased functionality of new component technologies that are created to meet the market demand of the computer and communications industries. Also the initial component costs are usually much lower than for the military counterparts.

4.1.2 Schematics

In order to maintain functional equivalence with the baseline military modules, the military schematics were used as the design baseline for the IBP-MPCL modules. The baseline schematics resided on HP workstations and were created in Mentor Graphics Design Architect. New parts were identified and submitted

to the ASD part librarian, and a separate library for the Marshall-AEN parts was created. Marshall-AEN part numbers were assigned to each of the commercial parts. The librarian created a pin map file, symbol, and geometry. When the parts library was fully populated, the schematic was revised with the updated parts.

For functions that were redesigned, the schematics were changed. The symbols created for the new parts had the same pin locations to aid in the schematic update. The DSP MCM was broken into discreet components. Seven schematic sheets had to be added to the "A" board design where the MCM was replaced. Each net name had to be changed and verified to obtain connectivity and signal names had to be checked for duplicates. A manual double-checking of signal net names was performed.

The schematics were prototype released as DV prefixed drawing numbers. Throughout the design verification process, changes were redlined on the drawing, and incorporation of revisions to DV prototype release drawings were given a numerical revision number. Upon completion of DV, all the changes were incorporated and the schematics were fully released for PV.

4.1.3 Part Specification Documents

The part specification documents for the Industrial Base Pilot program generally fell into three basic categories. These categories were existing AEN specifications, standard (off-the-self) microcircuits and custom (ASD Designed) microcircuits.

Existing AEN specifications included the component drawings that were already part of the TRW Automotive system. Primarily, these included passive components such as resistors, capacitors and inductors.

Most of the microcircuits used in the IBP-MPCL module designs were not currently in use by existing automotive electronic designs. For these standard microcircuits, new component drawings were created using the existing AEN drawing format and assigned AEN drawing numbers.

ASICs were assigned AEN part numbers, and were controlled and released through the AEN system. Baseline military program VHDL was reused and magnetic media was controlled and released at TRW ASD.

4.2 Design Development Testing

4.2.1 Parts & Reliability Testing

Surface-mount plastic encapsulated microcircuits (PEMs) are used in commercial and industrial electronics designs, primarily for their availability, cost, and size advantages. They are easily adaptable to automated assembly operations. As a result of their application in commercial communications systems and automotive electronics, many improvements have been made in package molding compounds to better withstand the environmental extremes of temperature and moisture.

Today's military avionics designs, with requirements for high reliability, reduced size and low weight, were chosen to take advantage of these improvements in the industrial microcircuit technology base, wherever possible.

The IBP-MPCL Component Reliability (CR) testing focused on thermal cycling and moisture susceptibility of plastic encapsulated microcircuits for use in military avionics digital processor modules. Today's avionics designs often use low profile Standard Electronics Module-Size E (SEM-E) modules, which preclude the use of through-hole microcircuit technology. This fact pushes the design selection of microcircuits to surface-mount, thin small outline packages (TSOPs), small outline J-leaded (SOJ) packages and Plastic Ball Grid Array (PBGA) packages.

For this program, two series of accelerated tests were conducted for the purpose of evaluating the moisture and temperature cycling susceptibility of standard as well as custom, plastic encapsulated microcircuits. The first group (hereafter referred to as CR1) consisted of 1248 commercially available plastic integrated circuits (ICs), representing 19 different part types from 9 different manufacturers. The second group (referred to as CR2) included 17 custom Application Specific Integrated Circuits (ASICs), and a mix of standard microcircuits that were not included in the CR1 test group. All of the above microcircuits were pre-conditioned by reflow solder-attach to test circuit boards on an AEN assembly line. The test boards were then subjected to a series of accelerated tests for the purpose of evaluating thermal cycling and moisture susceptibility of the plastic SMT ICs.

Figure 4.2.1-1 is a picture of a fully assembled test board from CR1 showing the nineteen different CR1 microcircuits that were chosen as candidates for the thermal and moisture accelerated testing evaluation. A picture of an assembled CR2 is shown in Figure 4.2.1-2. The commercially available devices selected

had to meet the form, fit and function requirements of current military avionics module designs. All these devices were surface-mount plastic encapsulated packages with either gull-wing leads or J-leads. Lead pitches ranged from 0.5mm (.020 inches) to 1.27mm (.050 inches) and the overall package heights were no greater than 3.8 mm (.150 inches).

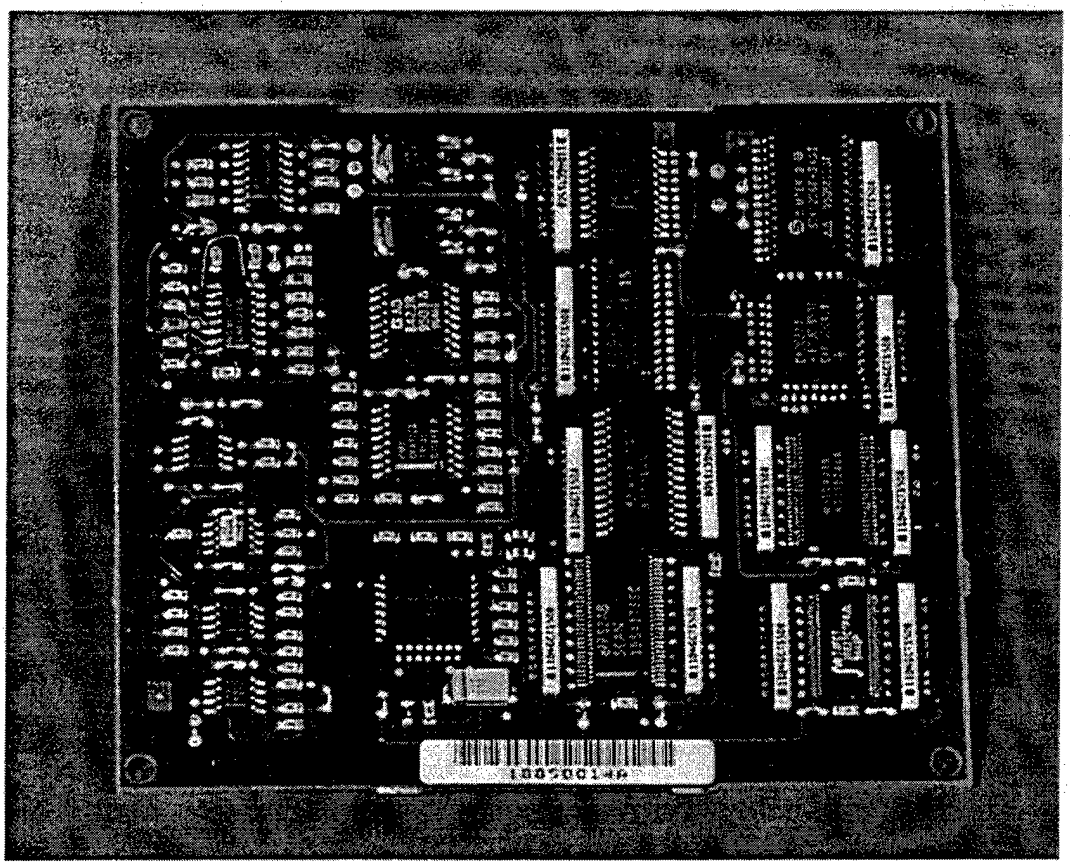


Figure 4.2.1-1 CR1 Test Board

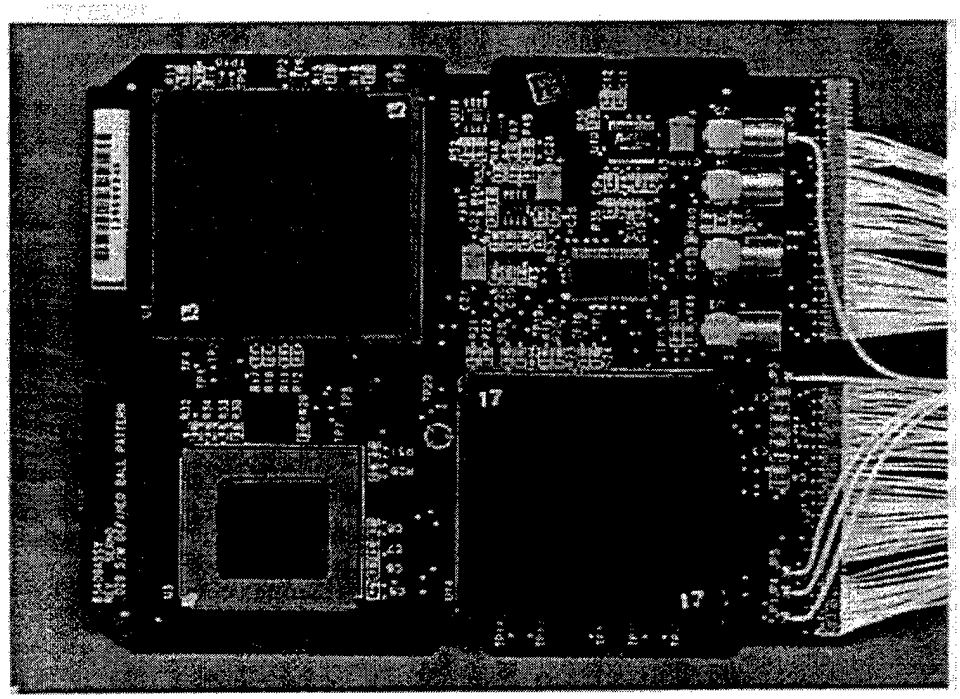


Figure 4.2.1-2 CR2 Test Board

CR2 test samples were subjected to a similar accelerated test sequence as CR1. A total of 80 standard commercial microcircuits (20 each of five different part types) and 17 custom DSP ASIC devices in Plastic Ball Grid Array (PBGA) packages were tested.

4.2.1.1 Manufacture of Test Boards

High temperature (180°C rated Tg) BT epoxy circuit board material was selected as the test carrier for the microcircuits. The primary purpose of mounting the devices on circuit boards was three-fold: First, to provide a preconditioning that was representative of actual manufacturing conditions; Second, to allow probe testing from the backside of each board by means of a bed-of-nails test fixture at a GENRAD test station; Third, to avoid design of sockets and programs that were not readily available to test all the device types individually. The CR2 microcircuits were wired out to solder pads on the edge of each test board as the large number of signal pins required to test the custom devices made it impractical to route test points through vias for the purpose of backside probe testing.

Prior to the solder reflow operation the devices were subjected to a 24-hour bake at 40°C, to minimize the risk of package rupture due to rapid moisture expansion

during the reflow temperature exposure. This is not standard procedure for a high volume automotive electronics production line.

Moisture sensitive components are normally received in protective packaging from the part manufacturer. The level of production is usually such that the components are exposed to room ambient conditions for only a short period of time prior to actual reflow attach. However, the relatively small quantity of components selected for this test had been removed from their packaging for an extended period of time and the actual levels of moisture absorption into the microcircuit packages were unknown.

The initial recommendation was to perform a higher temperature bake (90C to 125C) over a 24-hour period to insure the removal of absorbed moisture from the plastic molding compound of the device packages. When the initial group of devices were subjected to this bake while in their original packing containers, the elevated temperature damaged the container material. Consequently, the bake temperature was lowered to 40°C, but the bake time was left at 24 hours. This left packages at risk of delamination during reflow.

The solder reflow operation for the test boards was performed on an automated line normally used to assemble automotive electronics circuit boards.

The critical parameters of the solder reflow profile used for the test boards were:

1) +220°C maximum channel temperature.

2) 1.9°C per second preheat rise rate.

3) 79 ±3 second liquidus time (time above +183°C).

4) 158±10 second soak time (time at +150±10°C).

Following reflow component attach, the circuit boards were visually examined for defects and then electrically tested at room ambient (+23°C).

Accepted boards were segregated into three groups for conformal coatings of silicone, parylene and no coating. The purpose of incorporating conformal coatings in the experiment was to evaluate their effectiveness in minimizing package lead corrosion.

The back (non-component) side of the CR1 boards was left uncoated to allow the bed-of-nails test head at the GENRAD test station to make contact with the device test points on the bottom of the boards. Similarly the connection pads on the edges of the CR2 boards were masked to allow for the solder connection of test wires.

4.2.1.2 *Experimental Procedure*

The accelerated test sequences for each group of test boards (CR1 and CR2) are shown in Figures 4.2.1.3.1-1 and 4.2.1.3.1-2, respectively.

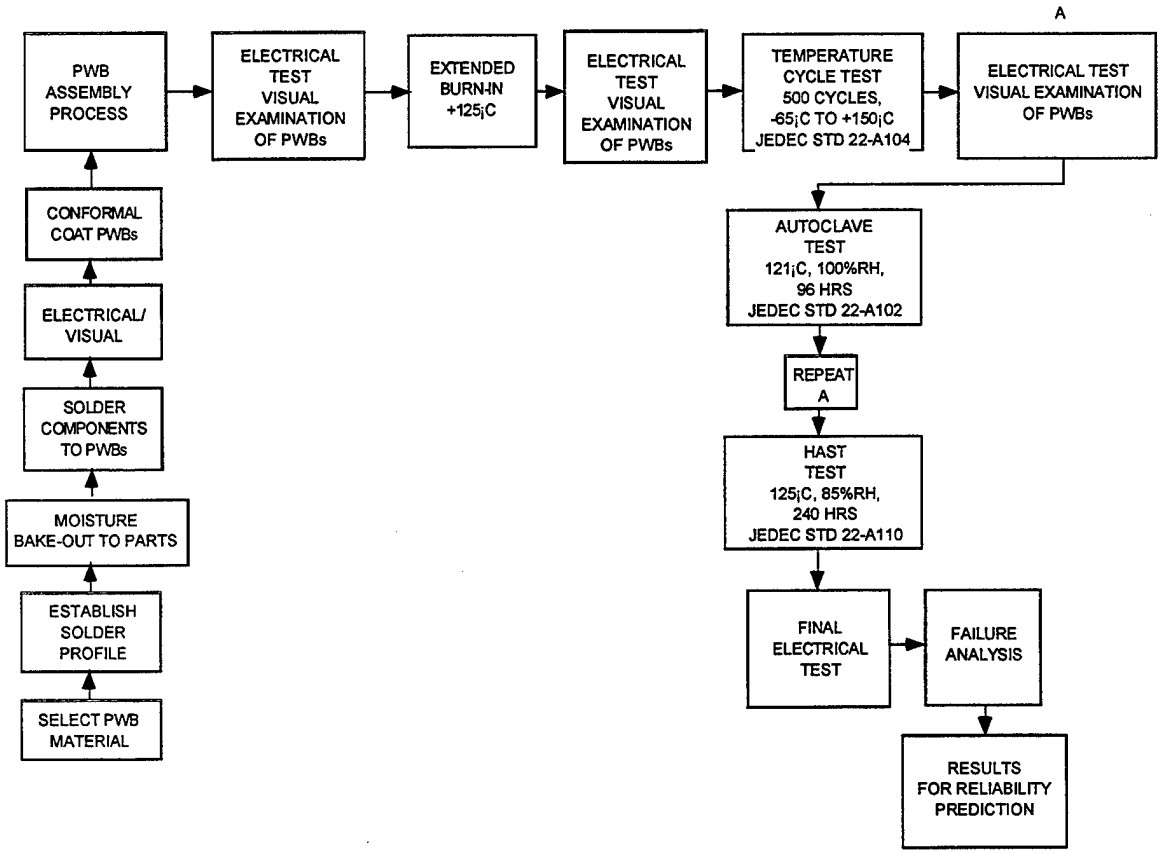


Figure 4.2.1.3.1-1 CR1 Test Flow

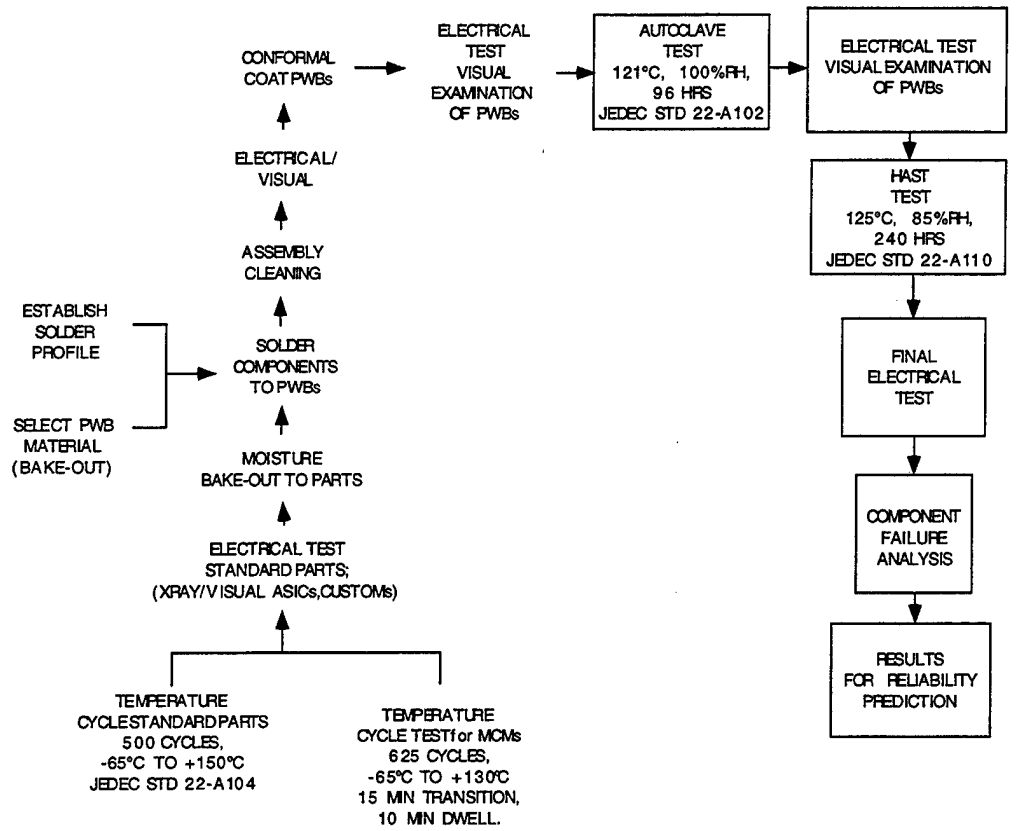


Figure 4.2.1.3.1-2 CR2 Test Flow

4.2.1.3 Test Results.

4.2.1.3.1 CR1

34 of the original 69 boards passed final parametric testing with no microcircuit failures. The 35 remaining boards had 91 microcircuits that did not pass parametric testing. A decision was made to remove these microcircuits from the remaining failed boards and test each microcircuit individually. The intent was to eliminate any variables associated with previous circuit board failures (open vias, resistors, fractured solder, etc.).

To accomplish this task, some devices (11) were bench tested in-house, where test fixtures were available and the remaining (80) devices were sent to the original manufacturers for functional testing.

At the conclusion of all the microcircuit testing (both on and off the boards), 7 confirmed microcircuit failures were identified.

4.2.1.3.2 CR2

79 out of 80 of the standard off-the shelf plastic encapsulated microcircuits passed functional testing following the environmental test sequence. The one device failure was an op amp which failed functional electrical testing following temperature cycle testing.

10 of 17 custom DSP ASICs passed the final functional test. The remaining 7 exhibited incorrect test patterns. 3 of the seven (representing the 3 unique failure conditions) were submitted for failure analysis.

4.2.1.4 Failure Analysis

4.2.1.4.1 Failure Analysis Plan

Each of the devices verified to be failures by the above criteria were submitted for analysis. Figure 4.2.1.5.1-1 describes the approach taken for the failure analysis.

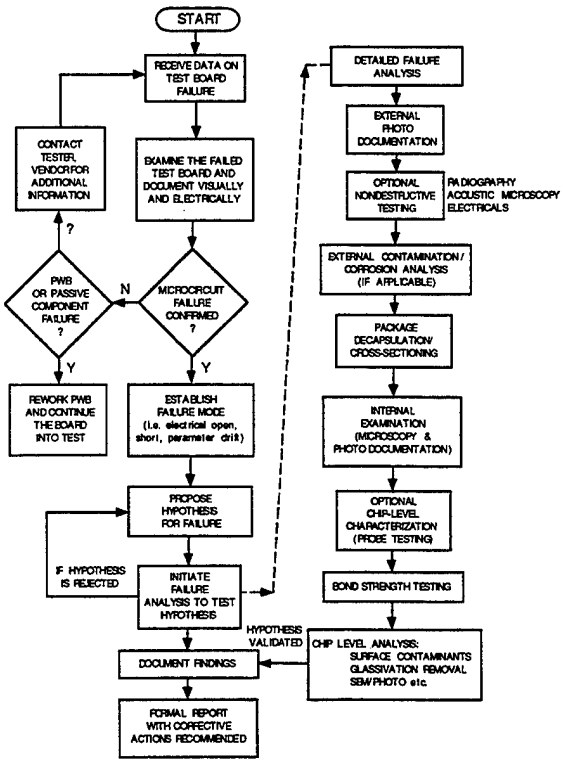


Figure 4.2.1.5.1-1 Failure Analysis Flow

4.2.1.4.2 CR1 Analysis Results

Seven devices were submitted for failure analysis after exposure to CR1 test environments and are described in the sections below. These sections address the details associated with the determination of the failure modes and failure

mechanisms associated with each of these devices. The devices are summarized below.

4-Maxim Comparators (MXL1016)

- Failed on boards: 5C, 7C,13B(after burn-in) 12B(after HAST)
  - -- 5C: -V shorted to Gnd, could not power up
  - -- 7C,12B,13B: no change in outputs as inputs are changed

1-Analog Devices Quad Op Amp (OP471GS)

- Failed on board: 21A(after autoclave)
  - -- Output B stayed at 4V when both inputs were grounded or when 500mV was applied.

2 - IDT 20 Bit Buffers (IDT74FCT16827CTPA)

- 1 Failed post burn-in functional testing (7C)
- 1 Failed parametric testing (5A)

Only 1 of the seven devices (U7 op amp/board 21A) had a failure mechanism (corrosion) that was attributable to moisture infusion from the environmental testing (autoclave).

As a consequence of this, an alternate device type was selected and the original failed part type was removed from design consideration.

The 6 remaining failures were most likely attributable to thermally generated bond intermetallics and current density driven metal migration as a result of over-accelerated conditions during the extended burn-in.

4.2.1.4.2.1 Parts Failing After Burn-in

There was no visual evidence of any through-package cracking. Acoustic microscopy was used to look for package delaminations. No delamination or internal cracking was observed on these parts. X-radiography showed no evidence of broken, shorted, or lifted bondwires.

The first of four failed comparators was cross-sectioned through the bondwires on die bond pads. An excessive amount of intermetallic growth was found on the bond pads, when compared with a "good" bond pad that was not exposed to the burn-in stress. This condition most likely contributed to a weakening of the bond and an eventual open circuit. Figure 4.2.1.4.2.1-1 shows an example of the intermetallic growth.

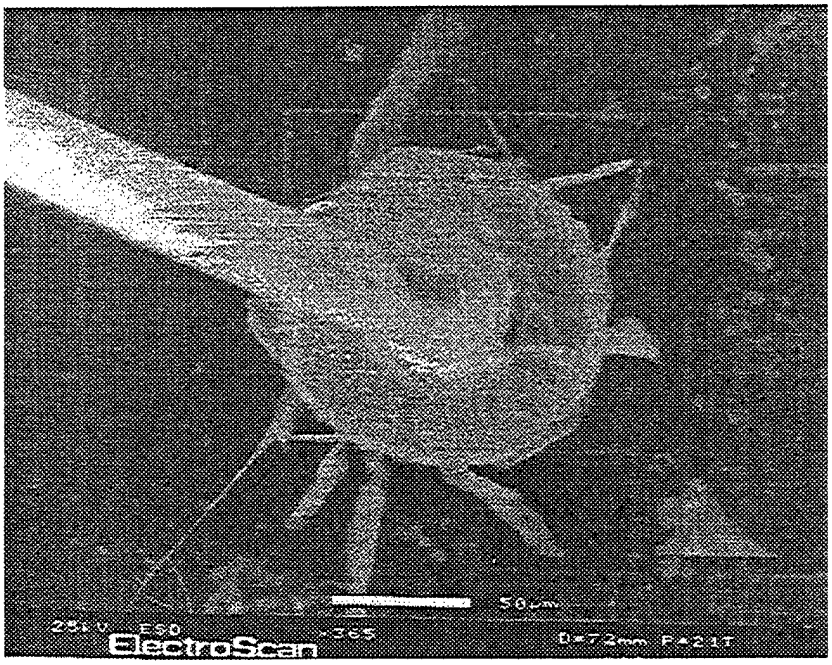


Figure 4.2.1.4.2.1-1 Comparator U19, Board 5C Intermetallic Growth

Given the lack of any other physical or electrical damage, the excessive intermetallic condition at the wirebond-bond pad interface was the most probable failure mechanism.

Two other comparators that failed were chemically decapsulated and did not show intermetallics. However, an examination of the die metallization traces revealed hillock and void formation, predominantly seen at the ends and corners of metallization traces. This condition was primarily due to either thermally induced stress relief or current density driven electromigration.

External examination and non-destructive acoustic and X-ray scanning revealed no evidence of cracks or delaminations in the plastic encapsulant material, and no lifted, broken, or shorted bondwires.

Based on this analysis, the short was most probably attributed to the resulting die metal hillock formations.

A 20 bit buffer also failed immediately after burn-in. Here again, there was no evidence of package cracking or delamination and no broken, lifted, or shorted bondwires. Decapsulation did reveal evidence of excessive intermetallic formations emerging from under the ball bonds. EDX analysis determined the formations to be composed of gold and aluminum. In addition to this, lower than average ball bond shear strength of 100g was observed.

4.2.1.4.2.2 Part Failing After Autoclave

A quad op amp failed test following autoclave. A mechanical decapsulation was performed on this part to minimize the loss of any potential corrosion artifacts that could occur with a chemical method of decapsulation.

The scanning acoustic microscopy revealed the presence of delamination on the top of the die. X-radiography showed no evidence of broken, shorted, or lifted bond wires.

Two other control op amps were mechanically decapsulated along with the failed device. The first control had also been exposed to autoclave, but exhibited no delaminations. The second control had not been exposed to autoclave. The failed sample (shown in Figure 4.2.1.4.2.2-1) had significantly more corrosion at the bond pads than either of the two controls (shown in Figure 4.2.1.4.2.2-2). Also, the ball bonds were so weakened by the corrosion that most were pulled off the failed sample during the mechanical decapsulation, but most of the bonds remained on the control samples during the decapsulation.

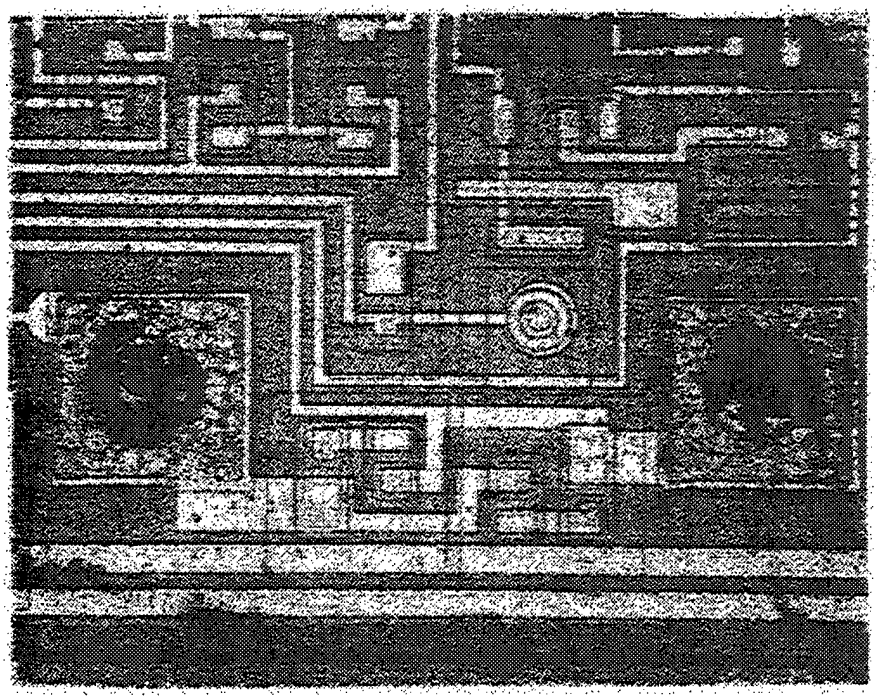


Figure 4.2.1.4.2.2-1 Op Amp U7, Board 21A Showing Bondpad Corrosion

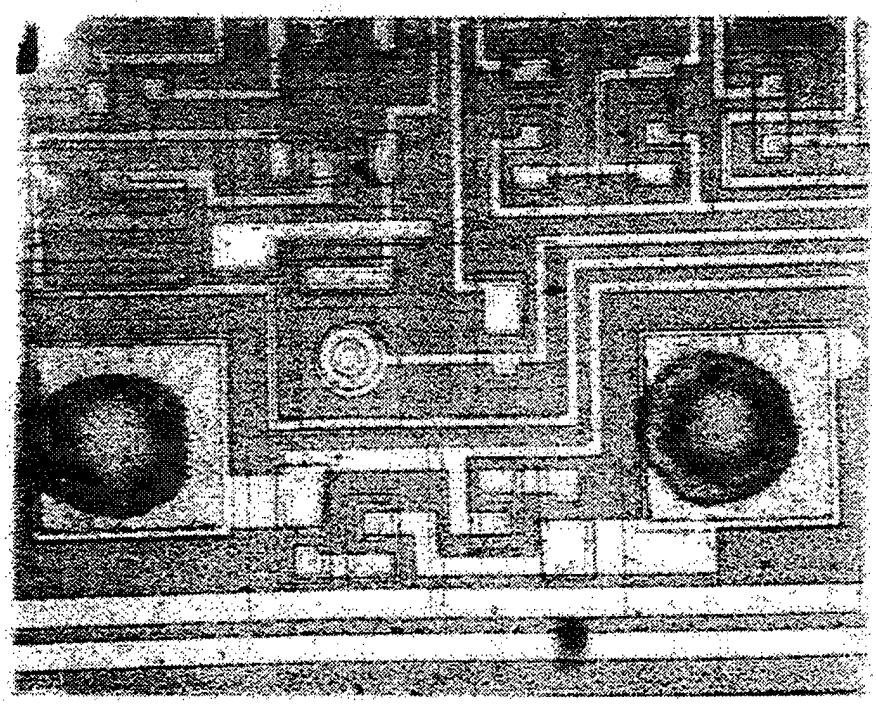


Figure 4.2.1.4.2.2-2 Op Amp Control Sample (showing no corrosion)

4.2.1.4.2.3 Part Failing After HAST

A fourth comparator failed after HAST testing. The failure mode was similar to that seen in parts that failed from burn-in stress alone. It was postulated that, even though this device was exposed to humidity and temperature in autoclave and HAST, it probably also failed due to an open circuit at the input pins due to excessive intermetallic formation at the bond pads. The fact that the part did not fail immediately after burn-in, as was the case with the other comparators, was attributed to reduced burn-in exposure (159 hours of burn-in instead of 525 hours). Destructive physical analysis did in fact reveal the presence of excessive intermetallic formation.

Another condition present was silver dendritic growth between the bondpads (see Figure 4.2.1.4.2.3-1). Further evaluation revealed that this resulted from a residual reaction with the silver die attach epoxy during the chemical decapsulation.

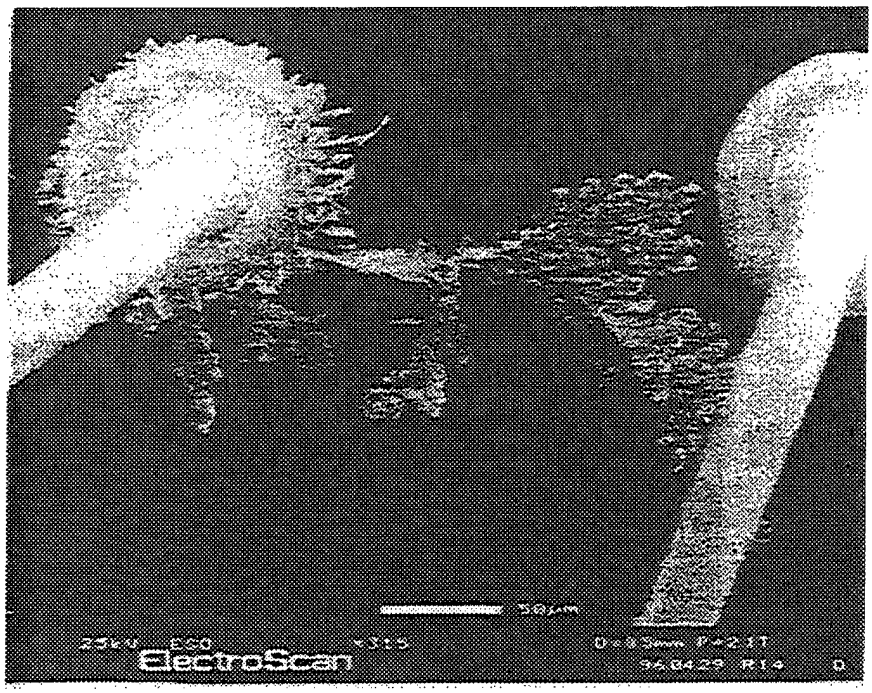


Figure 4.2.1.4.2.3-1 Comparator U19, Board 12B, Silver Dendritic Growth

4.2.1.4.2.4 Parametric Test Failure

An additional 20-bit buffer failed when resubmitted to the part manufacturer for functional test, after autoclave testing. It was not clear that this failed condition was the result of the accelerated test, since the device was not tested to the manufacturer's detailed test specification initially. An analysis was performed to examine the condition of the device.

There was a limited amount of lead corrosion at the trimmed ends of the leads and at the interface to the package due to exposed copper and absence of plating at these locations. There was no visual evidence of package cracking. Acoustic microscopy and X-ray yielded no evidence of delamination or bondwire failures.

The chemical decapsulation and SEM revealed traces of intermetallic growth under the ball bonds (see Figure 4.2.1.4.2.4-1).

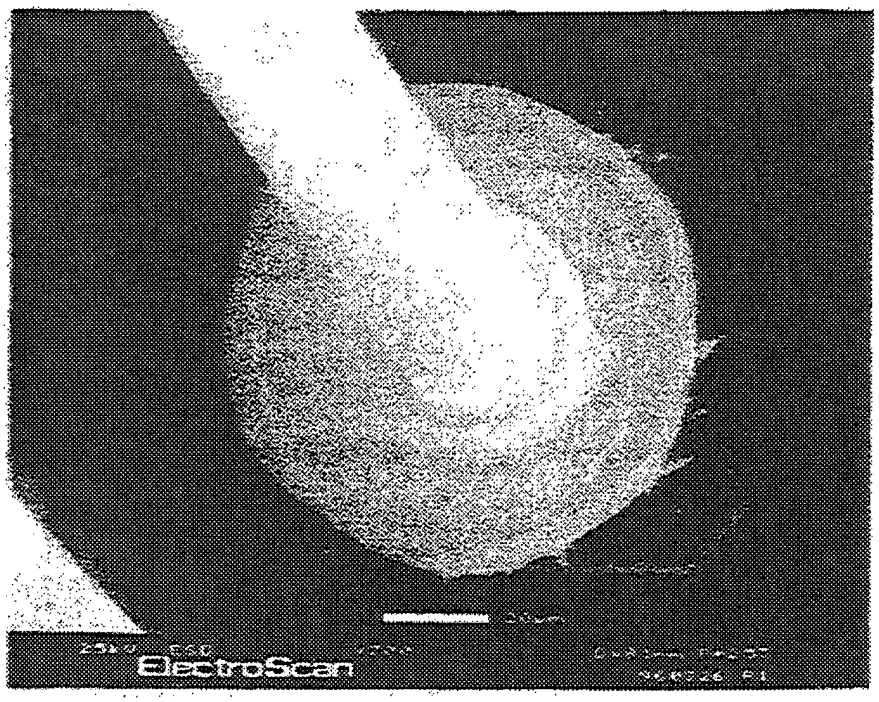


Figure 4.2.1.4.2.4-1 20 bit Buffer U15, Board 5A, Intermetallic Growth

Subsequent ball shear testing revealed that the bond had an acceptable, but somewhat weakened, bond strength of 101 gram average force. The intermetallic formation could eventually be responsible for changes in contact resistance leading to the parametric shifts.

4.2.1.4.3 CR2 Analysis Results

Failure analysis was performed on the op amp that failed electrical test after 500 temperature cycles from -65°C to +150°C. Visual examination of the device revealed no external lead corrosion and no external package damage. Subsequent acoustic microscopy revealed no evidence of delamination or cracking.

X-radiography revealed wire sweep from manufacturing which brought the wires to pins 5 and 6 perilously close together. This was confirmed by subsequent chemical decapsulation and SEM examination in which wires 5 and 6 appear to be touching each other. This wire contact would account for the failure condition observed.

There are two possible reasons for the wire-to-wire contact. The most likely reason is the wires were in contact as a result of wire sweep that occurred during the transfer molding process. This would have caused the device to fail an initial electrical test as well as the post-temp cycle test. The device

manufacturer performs sampling based electrical screening. Since an initial electrical test was not performed, failure before the temperature cycling cannot be ruled out. The other possibility is that wire sweep during the manufacturing process brought the wires close enough that they were later allowed to touch, either as a result of wire fatigue or sagging from the repeated temperature cycles. This type of failure mode is more likely in open cavity parts, than in plastic encapsulated parts.

The presence of the initial manufacturing defect caused the failure, not the environmental testing. Acoustic Microscopy or testing would screen out this particular defect condition.

Analysis was performed on the failed custom DSP PBGAs. Acoustic microscopy was used to evaluate the encapsulant material for any evidence of delamination or cracking following the CR2 test sequence. Some evidence of delamination (approx. 5% die surface area) was found on the DSP samples from boards 3A and 10B. The delamination occurred at the corners of the die, at the die surface/encapsulant interface. Following the decapsulation of DSP packages, the die were examined for evidence of corrosion or corrosion by-products resulting from moisture intrusion. No corrosion was found, but there was some evidence of oxidation on the bonded and unbonded die pads of the DSPs. Subsequent EDX evaluation revealed the oxidation to be aluminum oxide. A Focused Ion Beam (FIB) cross-section and EDX scan was performed on one of the wirebonds in the DSP. The presence of a thin interlayer of oxide at the wirebond/bondpad interface indicated the oxide to be a pre-existing condition, prior to encapsulation or environmental testing. Further investigation of DSP die and all related die in stores did not show this condition. The oxidation is presumed to have occurred at some time during the pre-encapsulation phase of device manufacturing.

It was determined that the DSP samples used for this testing were not manufactured with the same equipment and same controls as used for the production DSP devices. They were manually bonded with 1mil aluminum wire, versus the production devices that were automatically bonded with 1mil gold wire. The encapsulant material, die and packaging were the same as used in production DSPs.

Additional IBM PBGAs (RTP ASICs) were selected to undergo a sequence of testing and sonoscanning in order to identify when the delamination was occurring. Extensive evaluation of the PBGA manufacturing process ensued at the manufacturer as a result of these failures. Many corrective actions were put

in place that corrected the encapsulation and bonding defects found in these test devices.

4.2.1.4.4 Additional DPA

In addition to the analysis of the above device failures, components from 3 CR1 boards that successfully completed the environmental test sequence with no electrical test failures, were submitted for destructive physical analysis.

The results indicated no external evidence of package damage or corrosion. The evaluation did reveal a large percentage of the packages with delamination of the plastic encapsulant material over the surface of the die when analyzed by acoustic microscopy.

Table 4.2.1.5.4-1 summarizes the package delaminations in terms of percentage delamination of total die surface area, for each of the components on the 3 circuit boards (2B, 9A, 13B).

Table 4.2.1.5.4-1 Package Delamination Summary

PACKAGE	DEVICE	BOARD 2B	BOARD 9A	BOARD 13B	AVG. DELAM /DEVICE
SOP16	U18	93	93	99	95
PLCC32	U13	88	94	96	93
SOP16	U16	59	96	86	80
SSOP48	U9	28	88	95	70
FP3	U1	59	64	79	67
PLCC28	U4	98	63	26	62
SOP8	U12	38	74	61	58
FP3	U2	79	4	51	45
TSSOP56	U15	26	0	73	33
SOP16	U7	0	1	81	27
SOP16	U3	15	14	42	24
SOP8	U8	57	0	1	19
SOP8	U19	53	2	2	19
SOP28	U10	37	4	5	15
SOJ28	U5	10	35	0	15
SOP20	U17	0	1	18	6
SOP28	U11	4	1	8	4
SSOP56	U14	3	0	0	1
SOP8	U6	0	2	0	1
	AVG. DELAM/ BOARD:	39	33	43	-

In reviewing the data in Table 4.2.1.5.4-1, the degree of delamination appears to have little correlation with the type of package or the board tested. The most likely cause has been attributed to an insufficient pre-reflow bake (40°C/24hours). This fact, combined with the repeated rework thermal exposures to repair the boards between tests, is felt to be the primary contributor to the delamination.

The fact that all these devices passed their functional testing after being subjected to the above sequence of manufacturing, accelerated testing and rework cycles, is a good indicator of package robustness. To minimize or eliminate this delamination, the recommendation incorporated extended the low temperature bake time (i.e., 5 days at 40°C) or used a higher temperature bake (125°C for 24 hours). All plastic devices that have been exposed to an uncontrolled humidity environment prior to reflow or rework were baked.

4.2.1.5 Use Environment

The military avionics use environment is typically characterized by daily, time-limited, power-on operation over an extended lifetime (i.e., 20yrs, 12,000 op hours).

It is imperative to understand the baseline application environment prior to imposing accelerated tests on microcircuits. Under-acceleration may not adequately stress the devices to reveal the potential failures that could occur during normal life, whereas over-acceleration can result in failures that would not typically occur in the actual life of the product.

Typical characteristics of the military avionics environment include:

Operational profile:

* 8000 flight hours/20 years = 400 flight hours/ year avg.
* 4800 ground op hours/20 years = 240 ground op hours /year avg.
* Total operating hours/year = 640 avg.
* 640 op hours/8760 hours/year = 7.3% op time vs. 93% non-op time

Thermal Exposures:

* Diurnal (unbiased), -54°C to +58°C - 93% of the time (1490 cycles)
* Ground op (biased), -40°C to +85°C - 2.7% of the time (2668 cycles)
* Flight (biased), -40°C to +74°C - 4.6% of the time (5334 flights)

Humidity:

* Typically 50% of the time is above 80%RH

4.2.1.6 *Reliability Summary*

The testing for this experiment was performed serially. Consequently, the boards were subjected to the cumulative environments of extended burn-in, temperature, cycle, autoclave and HAST.

From a conservative point of view, and with the cumulative effect associated with the interactions of each test unknown, potential interactions were discounted and the reliability assessment for each accelerated test environment was evaluated separately.

The purpose of the testing was not to establish mean time between failures (MTBFs). So the tests were not carried to a median failure point. Instead, for the given sample sizes the testing was conducted until the predicted life for a given accelerated environment attained the duration required for the using environment (in this case 20 yrs). The stipulation was that all tested devices must pass the required tests. If a failure occurred in a given accelerated test and it was attributable to a failure mechanism of that test, then that particular device would be unacceptable for the corresponding using environment of the intended application.

Even though the small sample sizes and limited number of device-hours or device-cycles did not warrant a traditional reliability failure rate calculation, Table 4.2.1.7-1 summarizes the failure rate calculations for CR1 testing using currently accepted models (Chi-square and Poisson statistic). The results are also shown for a typical avionics lifetime. That this only establishes a starting point for an ongoing reliability monitor program where continuous data is accumulated and FIT predictions are continually recalculated, reflecting more accurate predictions of part lifetimes.

Table 4.2.1.7-1 Failure Rate Calculations

Accelerated Test:	TEMP CYCLE	AUTOCLAVE	HAST
Failures:	(None)	(U7)	(U19)
ACCELERATION FACTOR	12.7	1889	55
DEVICES/PART-TYPE INTO TEST	63	50	50
ACCELERATED TEST HOURS/CYCLES	518	96	240
DEVICE-HRS or DEVICE-CYCLES	32634	4800	12000
EQUIVALENT DEVICE-HRSor DEVICE-CYCLES AT USE CONDITIONS	4.14E+05	9.07E+06	6.60E+05
POISSON STATISTIC AT 60% C.L. (0 FAILS)	0.95		
POISSON STATISTIC AT 60% C.L. (1 FAIL)		1.95	1.95
FAILURE RATE (% PER 1000HRS or 1000cycles)	0.23	0.02	0.30
FITs	2292	215	2955
CHI-SQUARE AT 60% C.L. (0 FAILS)	1.83		
CHI-SQUARE AT 60% C.L. (1 FAIL)		4.04	4.04
FAILURE RATE (% PER 1000HRS or 1000cycles)	0.22	0.02	0.31
FITs	2208	223	3061
FAILURES/AVIONIC LIFETIME	.012 /5334 FLIGHTS	.03/20YRS	.04/12800 OP-HRS

Most of the damage observed during the course of the testing was to printed circuit boards, solder connections and the support bias components, not the microcircuits being evaluated. This was primarily due to the fact that the accelerated environments selected to test the microcircuits were excessive for the PWBs and the solder interconnections. Many of the HAST and autoclave equipment suppliers and test facilities recommend testing microcircuits using socketed boards with gold-plated solderless connections to avoid potential contamination by solder. This is the preferred approach a company should take to support an ongoing test program that plans to use PEMs in their future designs. The test carriers are reusable, more survivable and introduce fewer contaminants. The down side is that one must insure that devices receive the proper preconditioning in the form of time/ temperature exposures that reflect the eventual solder reflow profiles that will be seen in manufacturing.

4.2.1.7 Reliability Conclusions

The primary purpose of this testing was to obtain experimental data that would evaluate long term survivability of surface-mount PEM microcircuits for a specific military avionics application.

Most of the microcircuits tested exhibited no failures through the environmental test sequence performed. There were 7 CR1 device failures out of 1248 (.56%). All 7 were submitted for failure analysis to understand the failure mechanisms involved.

The test results support the justification for the use of plastic encapsulated device types for an application that had previously been limited to traditional ceramic, military part types. The selected surface-mount plastic encapsulated microcircuits that passed can be used in the avionics environment described herein.

This testing represents an initial qualification effort designed to validate the feasibility of using specific, commercially available plastic encapsulated microcircuits for a specific military avionics application. In order to utilize existing commercial / industrial technology for future military avionics applications, a continued effort must be made to evaluate each new part type for each application. Ultimately, part qualification and reliability data should be obtained from part manufacturers. However, if this data is not available or not adequate, then accelerated tests similar to the ones presented here are recommended.

4.2.2 Mechanical Development Testing

4.2.2.1 Characterization

Characterization testing was performed to obtain critical data that would ensure accurate analysis results. For low cycle fatigue durability analysis, the most critical parameter is component and board CTE. For high cycle fatigue durability analysis, the most critical parameter is module natural frequency. Tests to determine these parameters were performed and the results are described below.

4.2.2.1.1 CTE

Testing to determine coefficient of thermal expansion (CTE) for critical materials was performed. The primary values of concern were the CTEs of the composite module (boards bonded to cores) and the CTE of the parts. The difference of these two numbers is a primary driver in durability of solder joints under temperature cycling. The durability of this design is further complicated by the fact that plastic BGAs from different suppliers may use different encapsulating compounds and therefore will have different CTEs. This requires the CTE match of the module substrate to a multitude of unique component CTEs.

For the BGA components packaged and supplied by LSI, no mechanical equivalent was available. For this reason, getting good CTE data on LSI parts was critical so that data from durability testing could be extrapolated to

predictions of life capabilities for LSI parts. For this testing, 2 different size parts were instrumented on both top and bottom (A and B side, respectively). Gages were placed on both the center of the part and along one edge in the longitudinal and transverse direction. The results of this testing are shown in Table 4.2.2.1.1-1.

Table 4.2.2.1.1-1 CTE Measurements vs Temperature for LSI Parts

	LSI 313 (Center Gages)				LSI 313 (Edge Gages)				LSI 225 (Center Gages)				LSI 225 (Edge Gages)			
	Side A		Side B		Side A		Side B		Side A		Side B		Side A		Side B	
Temp	Long	Tran	Long	Tran	Long	Tran	Long	Tran	Long	Tran	Long	Tran	Long	Tran	Long	Tran
-37.5	5.4	5.2	8.4	10.3	12.7	9.9	13.6	13.5	5.7	7.3	7.8	9.0	10.4	8.9	14.7	13.1
-29.0	4.6	4.7	8.9	10.8	12.2	9.6	13.9	13.6	6.0	7.5	8.1	9.2	11.2	9.5	15.0	13.5
-12.5	3.8	4.1	9.4	11.2	11.6	9.2	14.1	13.7	6.2	7.7	8.4	9.4	12.0	10.0	15.2	13.8
12.5	3.3	3.5	10.2	12.1	11.1	8.5	14.9	15.6	6.2	8.4	7.9	9.8	12.6	10.7	16.3	13.9
37.5	4.1	4.6	10.7	13.0	12.1	9.7	15.6	15.4	8.1	10.2	8.5	10.0	15.7	13.2	16.7	14.7
62.5	4.7	5.4	11.5	13.9	11.2	9.6	15.8	15.7	8.3	11.5	7.7	10.2	16.9	15.3	16.8	14.1
87.5	6.0	7.0	10.9	13.5	10.8	9.5	15.4	15.0	12.0	15.0	17.6	14.9	17.3	15.5	16.2	14.4
112.5	5.9	7.4	11.3	14.2	12.6	9.6	14.7	15.4	13.8	16.3	10.8	12.1	18.0	15.6	15.5	13.6
137.5	7.3	8.9	12.6	14.4	16.0	11.9	15.2	16.1	14.3	17.1	11.9	13.5	17.4	15.7	15.7	13.7

Table 4.2.2.1.1-1 shows a wide variation in CTE depending on temperature, part size, direction and location on part. For durability analysis, engineering judgment was required to choose an appropriate value. Generally, the edge gages were chosen and the CTE was averaged over the use temperature range.

The other critical measurement for calculating durability is the CTE of the module. In order to simulate the proposed design solution, a module was made with BT/epoxy boards soft bonded to P120 cores. The results of the CTE testing are shown in Table 4.2.3.1.1-2. This shows that for most of the temperature range, the bonding material effectively decouples the board from the core and the CTE tracks that of the board alone. However, below about -33°C, the bonding material tends to couple the board to the core and the effective CTE is approximately that of the core material. This temperature corresponds with the glass transition temperature of the silicone adhesive selected for board to core bonding.

Table 4.2.3.1.1-2 CTE Measurements Module Substrate

	BT Epoxy Soft Bonded to P120			
	Side A		Side B	
Temp	Long	Tran	Long	Tran
-46.0	0.8	3.8	-2.5	1.0
-29.0	12.1	9.9	12.3	7.0
-12.5	14.4	15.6	14.9	12.6
12.5	15.3	17.6	15.8	15.3
37.5	15.3	18.1	15.8	16.8
62.5	17.4	20.1	18.2	19.1
87.5	17.4	19.5	18.5	18.8
112.5	16.2	18.3	16.2	16.7
137.5	14.6	14.8	14.4	13.6

4.2.2.1.2 Stiffness

The most critical parameter in determining the solder joint durability under vibration is the module natural frequency. In order to determine the expected natural frequency of the module, the core plate response was measured for a DV core under different configurations. The results of this testing are shown in Table 4.2.3.1.2-1. From this data, if it is assumed that the board assemblies add weight to the core plate without contributing to the stiffness, the module natural frequency is calculated as approximately 380 Hz. Because the boards do add stiffness, the actual natural frequency is expected to be approximately 500 Hz.

Table 4.2.3.1.2-1 Vibration Characterization Testing of DV Hardware

Configuration	Response	Fn	Q
Al/C-C core w/ wedgelocks	Core	834	34.2
Al/C-C core w/ wedgelocks and connectors	Core	783	45.8
Al/C-C core w/ wedgelocks, connectors and Gr/Ep covers	Cover B	236	3.4
Al/C-C core w/ wedgelocks, connectors and Gr/Ep covers	Core	735	Meas on Cover
Al/C-C core w/ wedgelocks, 1/2 connector and Gr/Ep covers	Cover B	247	3.6
Al/C-C core w/ wedgelocks, 1/2 connector and Gr/Ep covers	Core	742	22.6
Al/C-C core w/ wedgelocks, 1/2 connector	Core	619	12.4

4.2.2.2 Durability Testing

In order to develop a model to predict the fatigue life of ball grid array packages when exposed to vibration or temperature cycling, a pair of experiments were designed. The first experiment (DOE 1) was developed to define the manufacturing processes that result in a strong BGA solder joint. The second experiment (DOE 2) was developed to define the design parameters that reduce

the strain on the solder joints sufficiently to meet the durability life requirements. These experiments and limited results are described below.

One of the largest concerns in the IBP-MPCL redesign effort was the ability of the component interconnects to survive a lifetime of vibration and temperature cycling. The solder joints must be designed and built to withstand 20 years of the avionics environment. Critical environments include power cycling, temperature cycling and vibration. This 20-year environment can be compressed to a shorter time span (with equivalent damage effect) by increasing the stresses on the solder joint. Analytical models are used to correlate the compressed environments to the actual environment and predict the survivability over a 20-year life.

Data is available on the durability of some component types in the avionics environment. However, at the beginning of the IBP-MPCL redesign effort, there was insufficient durability data on the ball grid array packages, plastic packages, and some discrete packages that were candidates for use on the new designs. More data was needed on the design and process factors that influence survivability of interconnects in severe environments. It was decided to use Design of Experiment (DOE) techniques as a tool to determine the effects of these factors.

4.2.2.2.1 DOE Methodology

Design of Experiments is a technique that enables the effects of a number of design and process factors to be evaluated in an unbiased manner. This method minimizes the number of experimental replications needed to evaluate the effects of large numbers of factors. Through the use of Design of Experiments the significance of diverse factors on the survivability of solder joints could be determined at minimal expense.

The experimental plan was to first assemble representative parts onto circuit boards using DOE-specified combinations of process and design factors. Then the solder joints in the assemblies would be tested to failure using compressed environment cycles. Figure 4.2.3.2.1-1 shows the compressed thermal cycle used for the experiment. Figure 4.2.3.2.1-2 shows the vibration profile used for the experiment.

The goal of the experiment was to determine the best combination of factors that would maximize the life of the solder joints when exposed to vibration and thermal cycling. Failure of a joint was defined as any momentary electrical discontinuity.

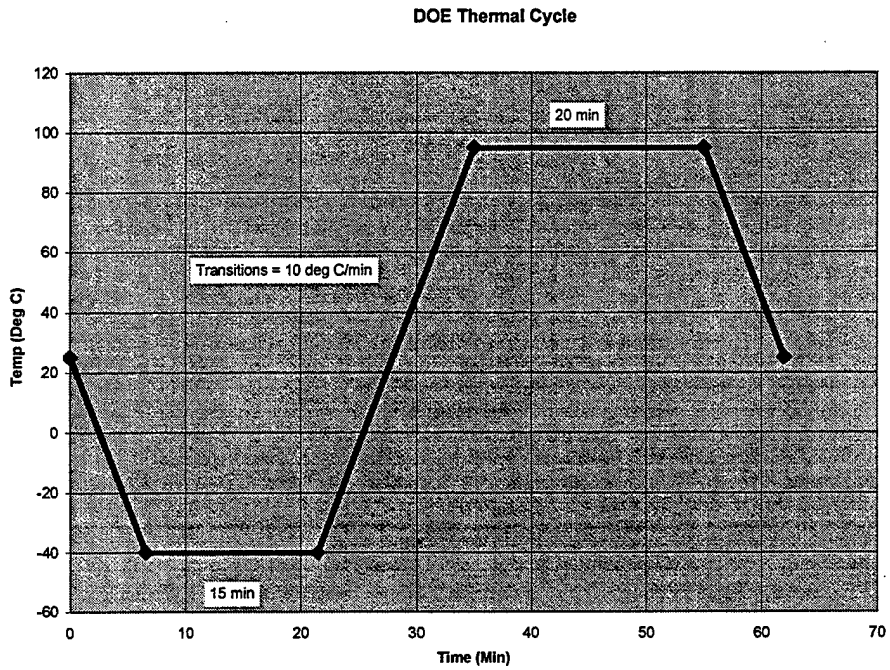


Figure 4.2.3.2.1-1 DOE Thermal Cycling Environment

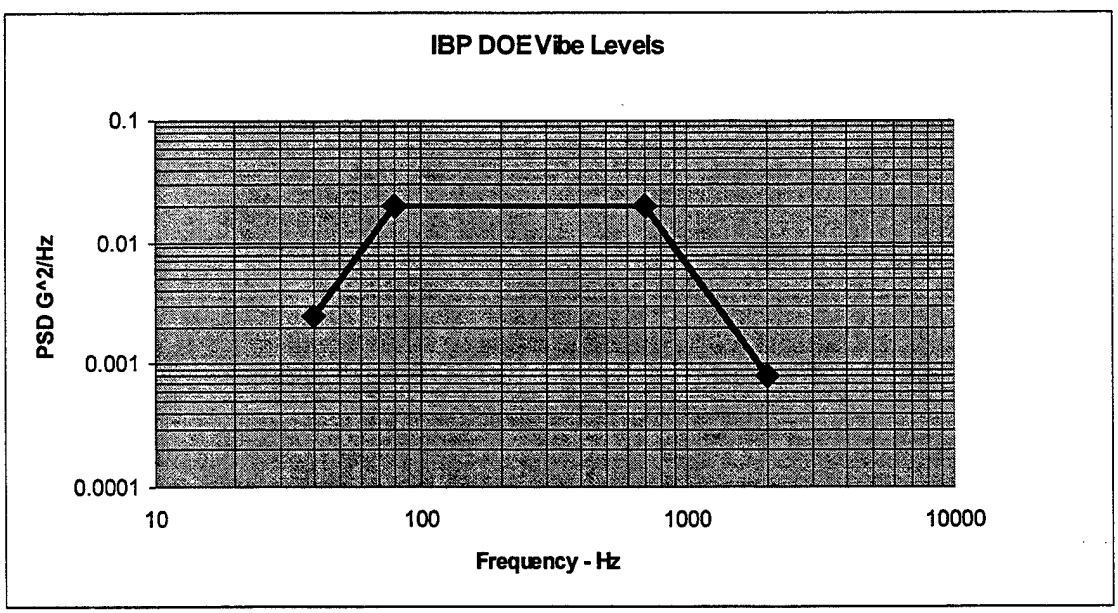


Figure 4.2.3.2.1-1 DOE Vibration Environment

The design of the experiment started out with a brainstorming process to collect a list of the possible effects on solder joint durability. The brainstorming sessions included mechanical design engineers, electrical design engineers, component engineers and process engineers. Once the brainstorming was

complete, consensus techniques were used to reduce the list to the factors considered the most relevant.

These factors fell into either of two major categories. One set of process and design factors affected the geometry and metallurgy of the solder joint. The other set of factors affected the amount of strain the solder joints would see, primarily from material properties of the module or part. Having both categories of factors in the same experiment could cause non-linear interactions. Non-linear interactions are difficult to deal with in a DOE and should be avoided.

It was decided to separate the experiment into 2 parts. The first was to be called DOE 1. It concentrated on determining the best mix of variables for making durable solder joints on each part. Once the durability of the joints was maximized, the second part of the experiment, called DOE 2, would concentrate on finding material properties for the thermal core, bonding adhesive, and circuit board laminate that would minimize the amount of strain on the solder joint when exposed to the compressed thermal and vibration environments. The parameters that were examined in DOE 1 were parameters that could be changed at a relatively low cost impact. The parameters that were examined in DOE 2 such as core materials had to be optimized for cost.

4.2.2.2.2 DOE 1 Experimental Design

Following the Design of Experiments guidelines, the factors under study in DOE 1 were further separated into 2 categories: control factors and noise factors.

4.2.2.2.2.1 Control Factors

Control factors are process and design factors that can be easily set or controlled. An example would be a machine setting or a design parameter. Eleven factors were selected for this experiment.

All of the factors chosen would possibly affect BGA solder joint durability. The design included J-leads, gull wings and LCCs as "controls". The other solder joints, such as those from J-leaded, gullwing or leadless parts, would not have the factors specific to BGA solder joints, such as solder ball size or composition.

The following is a list of control factors chosen for this experiment along with a description of the two levels chosen for each factor

Pad Size

The size of the pad affects the final geometry of the joint. The large and small sizes of pads were defined as either the same diameter as the solder ball, or .005

inches smaller. This factor was applied to BGA parts only, since pad sizes for the other parts in the study were well established.

Pad Definition

Some published studies have shown that solder joint life-expectancy of BGAs increases for pads that have their solderable area defined by the opening in the solder mask coating (the solder mask covers some of the outside diameter of the pad), instead of the usual uncoated pad. This factor was applied to BGA pads only.

Pad Plating

This factor was selected to study the relative effects of Enthone-coated copper versus the more traditional tin/lead plate and fuse solder coating on the solderable pads. This factor was in effect for all part types on the test boards.

Solder Ball Size

This factor only applied to the ceramic and plastic BGA561 part types. Other BGA package styles were not available in differing ball sizes and style. Reflowable solder balls were either .025 or .030 inches in diameter. The balls with higher melting points were .030 or .035 inches in diameter.

Solder Ball Material

Solder ball composition, like solder ball size, was only varied on the custom-built BGA561s. The two factors were Sn62Pb36Ag2 and Sn10Pb90. The Sn10Pb90 solder ball does not reflow at normal processing temperatures, thereby retaining their spherical shape.

Solder Paste Material

The experimental boards were paste-printed with either Sn63Pb37 eutectic solder, or an Indium alloy In60Pb40.

Solder Flux

The nominal level of this control factor was the standard flux available for the solder paste formulations: WS for the eutectic and RMA for the Indium alloy. The other level of this factor was the use of less aggressive no-clean formulations of each solder paste.

Paste Volume

The amount of solder paste deposited on the pads for each joint was varied by using either .006 or .008 inch thick stencils and by varying the size of the solder paste stencil apertures.

Reflow Profile

Under one manufacturing plan, the surface mount parts would be installed with the circuit boards already bonded to a thermal core. The resulting thermal reflow profile would have slower heating and cooling ramps. The nominal profile was set as suggested by the solder paste manufacturer. The alternative profile used a slower ramp rate to simulate the more massive core.

Second Reflow

Building the modules as a double-sided circuit board would necessitate having the first side of the module built to withstand a second reflow while in the inverted position as a part of the installation process of the second side. The nominal condition was one reflow cycle. The alternative level of the factor was a second reflow in the inverted position.

Conformal Coat

This variable was used to study the effect of conformal coat on the life of the solder joint. The conformal coat used was a silicone that had been selected as the standard for the AEN facility. The other level was to leave the board uncoated.

4.2.2.2.2.2 L12 Control Factor Array

The L12 Orthogonal Array was chosen as a best fit for the experimental situation. With this array, as many as 11 control factors having two different levels could be examined for relevancy. Aside from examining a large number of factors, another advantage to using the L12 array was the way the interaction effects between factors would be spread out throughout the result matrix. Data interpretation was clearer with only primary effects being studied. Care was taken to choose factors that did not have latent non-linear interactions.

The resultant L12 experimental array is illustrated in Table 4.2.3.2.3.2-1. The control factors are listed across the top, and each numbered row lists the correct levels of factors that went into making a circuit board assembly of that specific combination.

Table 4.2.3.2.3.2-1 L12 Control Factor Array

	Pad Size	Pad Definition	Pad Plating	Solder Ball Size	Ball Material	Solder Paste	Solder Flux	Paste Volume	Reflow Profile	Second Reflow	Conform Coat
1	large	Mask	Solder	small	Sn62	Sn63	nominal	less	extra mass	yes	no coat
2	large	Mask	Solder	small	Sn62	Indium	no clean	more	nominal	no	silicone
3	large	Mask	Copper	large	Sn10	Sn63	nominal	less	nominal	no	silicone
4	large	Clear	Solder	large	Sn10	Sn63	no clean	more	extra mass	yes	silicone
5	large	Clear	Copper	small	Sn10	Indium	nominal	more	extra mass	no	no coat
6	large	Clear	Copper	large	Sn62	Indium	no clean	less	nominal	yes	no coat
7	small	Mask	Copper	large	Sn62	Sn63	no clean	more	extra mass	no	no coat
8	small	Mask	Copper	small	Sn10	Indium	no clean	less	extra mass	yes	silicone
9	small	Mask	Solder	large	Sn10	Indium	nominal	more	nominal	yes	no coat
10	small	Clear	Copper	small	Sn62	Sn63	nominal	more	nominal	yes	silicone
11	small	Clear	Solder	large	Sn62	Indium	nominal	less	extra mass	no	silicone
12	small	Clear	Solder	small	Sn10	Sn63	no clean	less	nominal	no	no coat

4.2.2.2.2.3 Noise Factors

Conditions that either cannot be easily controlled or are left uncontrolled for reasons of cost or practicality are noise factors. Replicating a DOE to attempt to capture the entire range of each noise factor is not cost effective. Instead, the experiment is replicated with the extreme conditions of noise present in the experimental environment. Control factors that are least affected by noise are factors that can be counted on to produce stable processes and designs.

Coplanarity

From other studies and published material, it was determined that solder joint geometry, and fatigue life, can be greatly affected by the amount of warp in the BGA package and the board. However, the warp, or coplanarity can only be controlled within certain limits. The stack up of tolerances could potentially cause large variation in joint fatigue life.

For this reason the parts and boards to be subjected to thermal cycles were sorted into 2 groups. One group had the flattest parts, the other group had the most warped. Parts and boards that fell between the two extremes of warping were subjected to vibration cycling.

Part Location

The amount of strain each solder joint saw was a function of where on the board that part was located, particularly for vibration extremes. The DOE 1 boards were laid out so that each part type was replicated in a location near the center of the board, as well as a location near the edge of the board.

In DOE terms the table of results is known as a Response Table. Each package style in the experiment would have solder joints built with the 12 different combinations of control factors at each of 4 noise conditions for the thermal cycle test articles and 2 noise conditions for the vibration test articles.

4.2.2.2.3 DOE 1 Test Articles

The circuit boards for the test articles were 0.050 inch thick, 6 layer BT epoxy. Care was taken to include power and ground planes similar to copper planes on the boards to be used for the IBP-MPCL redesign. The board outline was also derived from the IBP-MPCL redesign.

Each assembled board was bonded to .050 thick aluminum core. Each core had 2 boards, one on each side. The adhesive used would tightly couple the circuit board to the aluminum, so that the assembly would experience thermal expansion near the rate of aluminum. Along with the compressed thermal cycles, the high coefficient of thermal expansion would accelerate failures, yielding data without prolonged testing.

The plastic part versus ceramic part design solutions were analyzed and found to be mutually exclusive. In order to match expansion coefficients between the board and the parts, a design would have to be either all ceramic BGA or all plastic BGA. Mixing the two technologies would not allow for a design solution. Separate modules for the ceramic and plastic parts were built.

Figure 4.2.3.2.4-1 shows the design of the circuit board with plastic parts on it. The circuit board populated with ceramic parts had a similar layout, with the same size BGAs, but some of the pin counts differed. The response tables summarize how long it took for each part to have a solder joint fail.

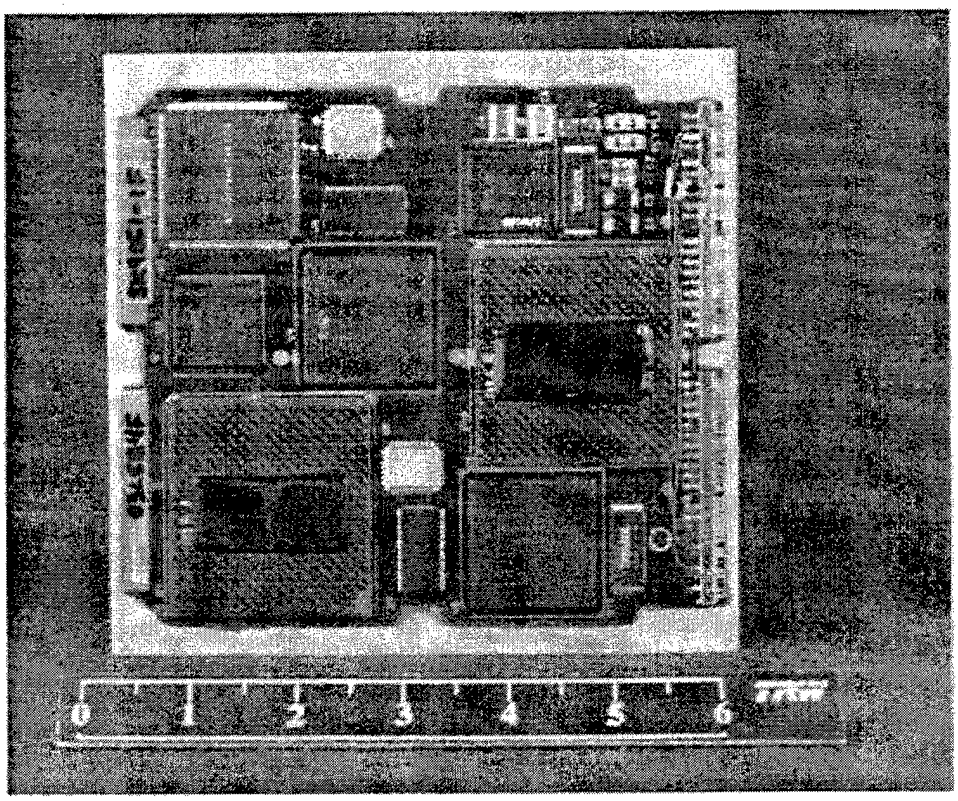
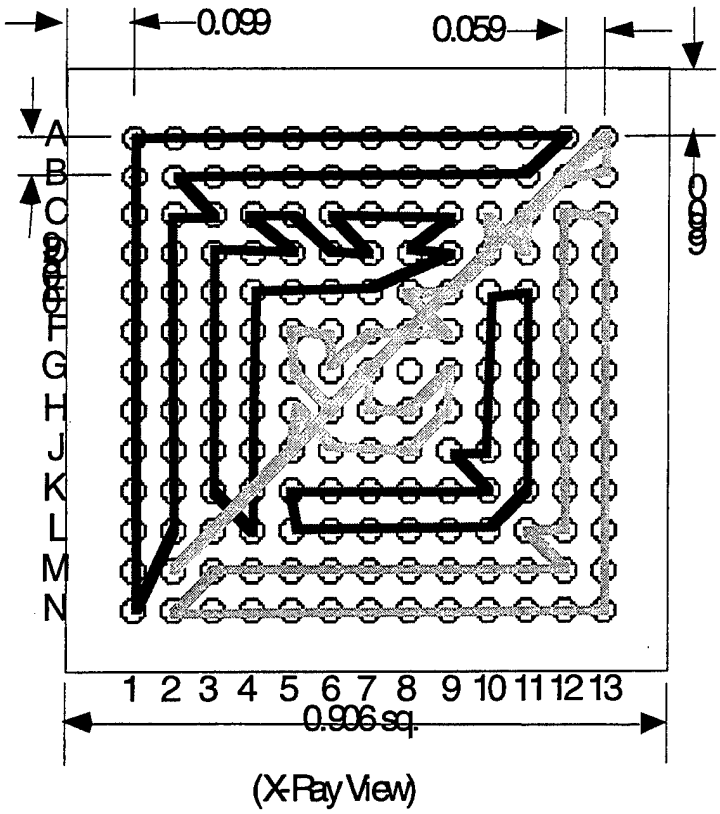


Figure 4.2.3.2.4-1 DOE 1 Board Design

On the test article circuit boards, solder joints were daisy chained together and connected to test equipment that captured each instance of discontinuity. The amount of test equipment needed to monitor the solder joint chains was kept to a manageable level by including as many as 50 solder joints in a chain sequence.

With this technique, the initial failure of a part could be tied to a specific solder joint chain on a part, but not to a specific solder joint within the chain. The chains were restricted to specific areas on each part, in order to facilitate failure analysis.

Figure 4.2.3.2.4-2 shows how the BGA169 package was subdivided into 5 chains. Other parts were subdivided in a similar ways. Table 4.2.3.2.4-1 shows the various part types on each DOE board, their pin count, and into how many chains each part was subdivided.



BGA169, Full Grid, 23mm Body, 1.5mm pitch

Figure 4.2.3.2.4-2 PBGA169 Chain Map

Table 4.2.3.2.4-1 DOE 1 Parts List

Part Style	Part Description	Leads / Spheres	Parts / Board	Chains / Part
PBGA169	23mm square plastic ball grid array	169	2	5
PBGA313	35mm square plastic ball grid array	313	2	7
PBGA561	52x54mm plastic ball grid array	561	2	11
CBGA256	23mm square ceramic ball grid array	256	2	5
CBGA625	35mm square ceramic ball grid array	625	2	7
CBGA561	52x54mm ceramic ball grid array	561	2	11
J32	J-Lead DIP .400 inch centers	32	2	2
CLCC32	ceramic leadless chip carrier .45x.55 inches	32	2	2
CDR35	1825 ceramic chip cap	2	2	1
CWR11D	2817 molded tantalum cap	2	2	1
Filter	2707 melf NFM61	3	2	1
Inductor	1210 molded chip inductor	2	2	1
Diode	1.6x3.5mm mini-melf SOD-80	2	2	1
TSOP32	19.7mil pitch thin small outline	32	2	2
QFP240	19.7mil pitch quad flat pack	240	1	4

4.2.2.2.4 DOE 1 Test Results by Package Style

For thermal cycling, two repeats of the L12 array were subjected to a maximum of 2000 cycles at -40°C to 95°C. Boards were hard bonded to aluminum cores to accelerate failures. The resulting cycles to first failure were entered into result matrices. Tests were halted at 2000 cycles. In order to calculate data, if a chain had not failed in 2000 cycles it was assumed to have failed at 2500 cycles.

For Vibration, one repeat of the L12 array was subjected to 6000 minutes of vibration at 70°C. Boards are hard bonded to aluminum cores to accelerate failures. The cycles to first failure were entered into result matrices. Tests were halted at 6000 minutes. In order to calculate data, if a chain had not failed in 6000 minutes it was assumed to have failed at 7500 minutes.

4.2.2.2.4.1 TSOP32

The TSOP32 survived the vibration tests in all combinations, but began to have significant numbers of failures halfway through the thermal cycling tests. The Response Table is shown in Table 4.2.3.2.6.1-1. The Factor Analysis for the TSOP32 is shown in Figure 4.2.3.2.6.1-1. The TSOP package is very light, with relatively thick leads at a 20 mil pitch. These parts showed a major positive

response towards using the creep-resistant Indium solder paste. It is likely that the thickness of the leads did not allow them to flex enough to reduce all the strain in the joints caused by thermal mismatches.

Table 4.2.3.2.6.1-1TSOP32 Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Left Part	Right Part	Left Part	Right Part	Left Part	Right Part
1	Intact	860	1199	1013	Intact	Intact
2	1338	1082	Intact	Intact	Intact	Intact
3	887	751	1007	1239	Intact	Intact
4	860	949	1019	527	Intact	Intact
5	1467	1467	1795	2000	Intact	Intact
6	1035	648	1324	720	Intact	Intact
7	1324	720	646	1044	Intact	Intact
8	718	Intact	899	Intact	Intact	Intact
9	1032	Intact	1970	1857	Intact	Intact
10	983	968	1302	1272	Intact	Intact
11	Intact	Intact	Intact	926	Intact	Intact
12	577	612	711	554	Intact	Intact

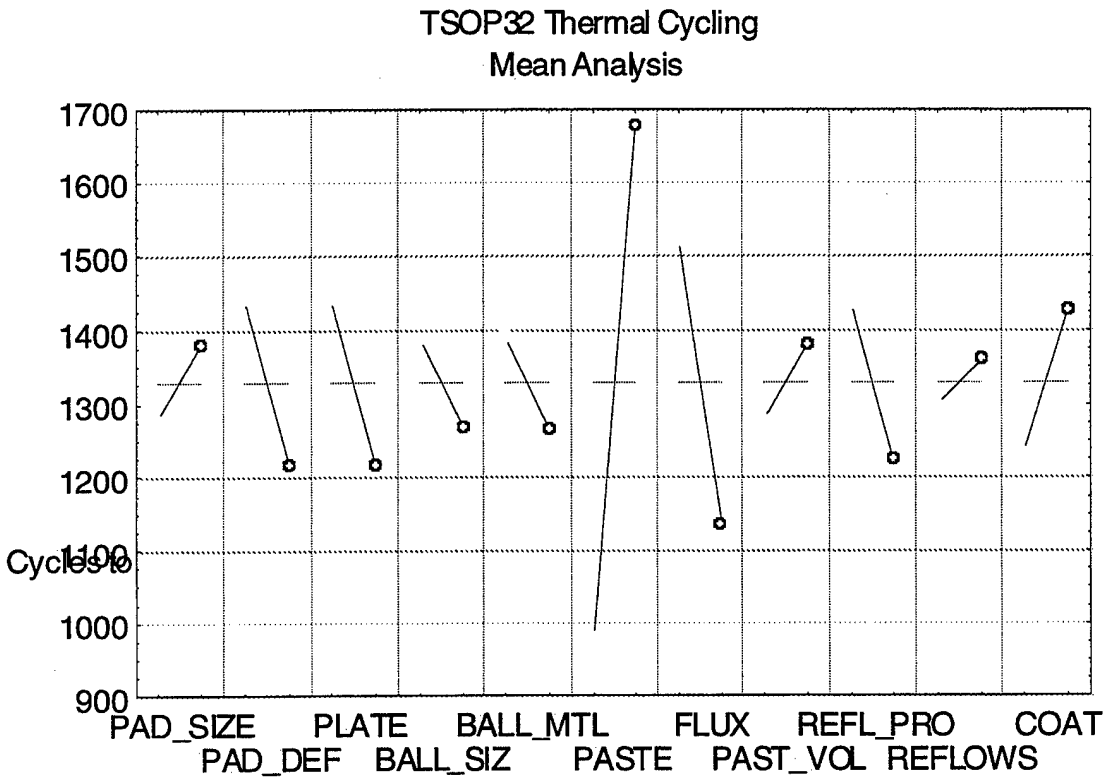


Figure 4.2.3.2.6.1-1TSOP32 Thermal Cycling Means Analysis

4.2.2.2.4.2 JLEAD32

The JLEAD32 survived the vibration tests in all combinations, and most of the parts subjected to the 12 factor combinations survived thermal cycling. The Response Table is shown in Table 4.2.3.2.6.2-1.

As expected, the J-leads provide a robust joint. There were some early failures caused by leads that were obviously damaged prior to part placement. With these failures removed from the response table, the remaining data is not significant enough to create a means analysis graph.

Table 4.2.3.2.6.2-1 JLead32 Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	Intact	Intact	Intact	Intact	Intact	Intact
2	Intact	Intact	Intact	Intact	Intact	Intact
3	184	Intact	Intact	Intact	Intact	Intact
4	Intact	Intact	1513	Intact	Intact	Intact
5	Intact	Intact	Intact	Intact	Intact	Intact
6	Intact	Intact	Intact	Intact	Intact	Intact
7	Intact	Intact	Intact	Intact	Intact	Intact
8	Intact	Intact	701	Intact	Intact	Intact
9	Intact	Intact	Intact	Intact	Intact	Intact
10	Intact	Intact	Intact	Intact	Intact	Intact
11	1608	Intact	Intact	Intact	Intact	Intact
12	Intact	Intact	Intact	1675	Intact	Intact

4.2.2.2.4.3 CLCC32

The CLCC32 packages survived the vibration tests in all combinations, but few of the combinations lasted past one thousand thermal cycles. The Response Table is shown in Table 4.2.3.2.6.3-1. The Factor Analysis for CLCC32 thermal cycling is shown in Figure 4.2.3.2.6.3-1.

The CLCC32 package was not expected to do well in thermal cycling because of the large difference in expansion rates between aluminum and the ceramic part. The primary reason this part was included in the study was because of the great deal of failure data on this package from previous solder joint durability testing. Data from this study was compared to failure data from previous testing to provide a measure of test control.

All the strain is absorbed in the solder joints. Accordingly, there were many early failures. There was a significant increase in cycles to failure from the use of the Indium-based solder.

Table 4.2.3.2.6.3-1 CLCC32 Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	75	75	132	132	Intact	Intact
2	364	660	305	1218	Intact	Intact
3	108	108	136	96	Intact	Intact
4	73	73	73	73	Intact	Intact
5	390	613	467	168	Intact	Intact
6	80	123	90	80	Intact	Intact
7	90	80	90	153	Intact	Intact
8	495	748	976	565	Intact	Intact
9	372	571	650	650	Intact	Intact
10	233	199	158	99	Intact	Intact
11	316	316	535	976	Intact	Intact
12	80	80	51	51	Intact	Intact

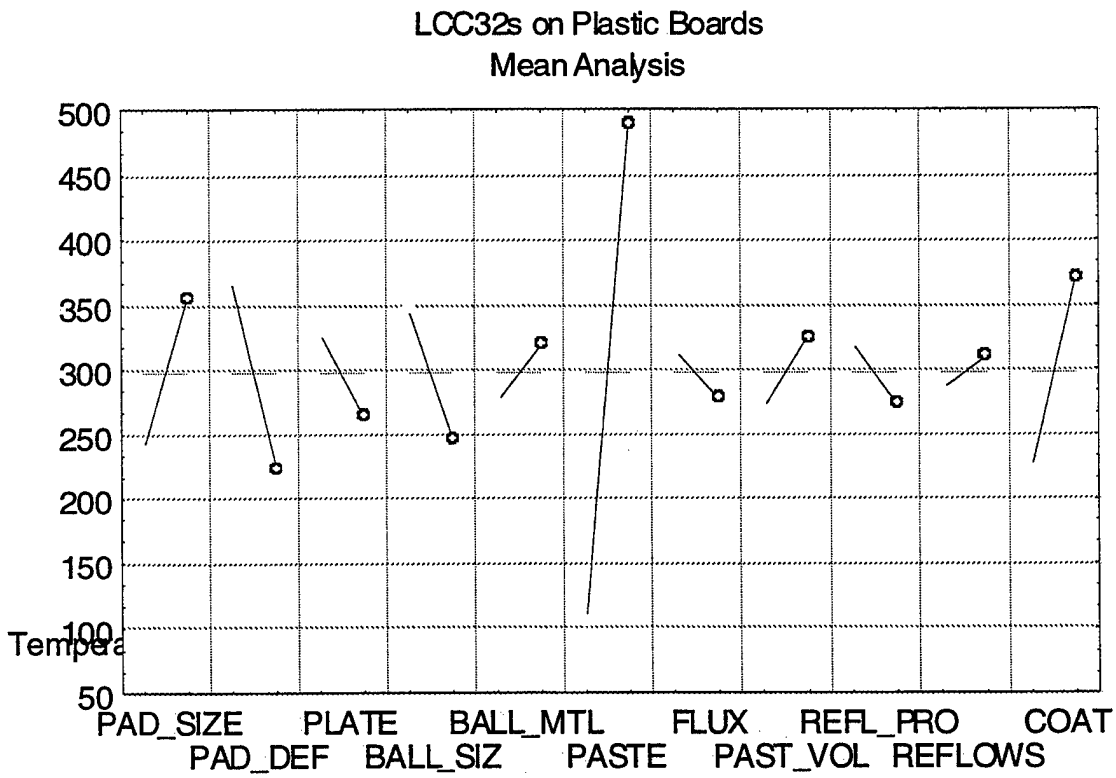


Figure 4.2.3.2.6.3-1 CLCC32 Thermal Cycling Means Analysis

4.2.2.2.4.4 PBGA561

The PBGA561 packages had a large spread of failure points for the 12 different combinations of factors. Although there were some early failures, half of the parts survived the full 6000 minutes of vibration. The Response Table is shown

in Table 4.2.3.2.6.4-1. The Factor Analysis for PBGA561 thermal cycling is shown in Figure 4.2.3.2.6.4-1. The Factor Analysis for PBGA561 vibration cycling is shown in Figure 4.2.3.2.6.4-2.

Table 4.2.3.2.6.4-1 PBGA561 Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	1806	1868	617	1263	1470	1020
2	524	1007	654	909	1800	Intact
3	607	1033	526	1294	Intact	Intact
4	1190	671	1032	870	1400	1400
5	613	1456	891	1319	4200	714
6	2500	1746	1418	1728	Intact	Intact
7	231	2500	579	1862	Intact	Intact
8	123	274	141	284	333	2800
9	457	523	324	168	1800	3600
10	1154	1806	751	1078	Intact	Intact
11	374	2500	747	2500	Intact	Intact
12	153	90	34	34	1800	Intact

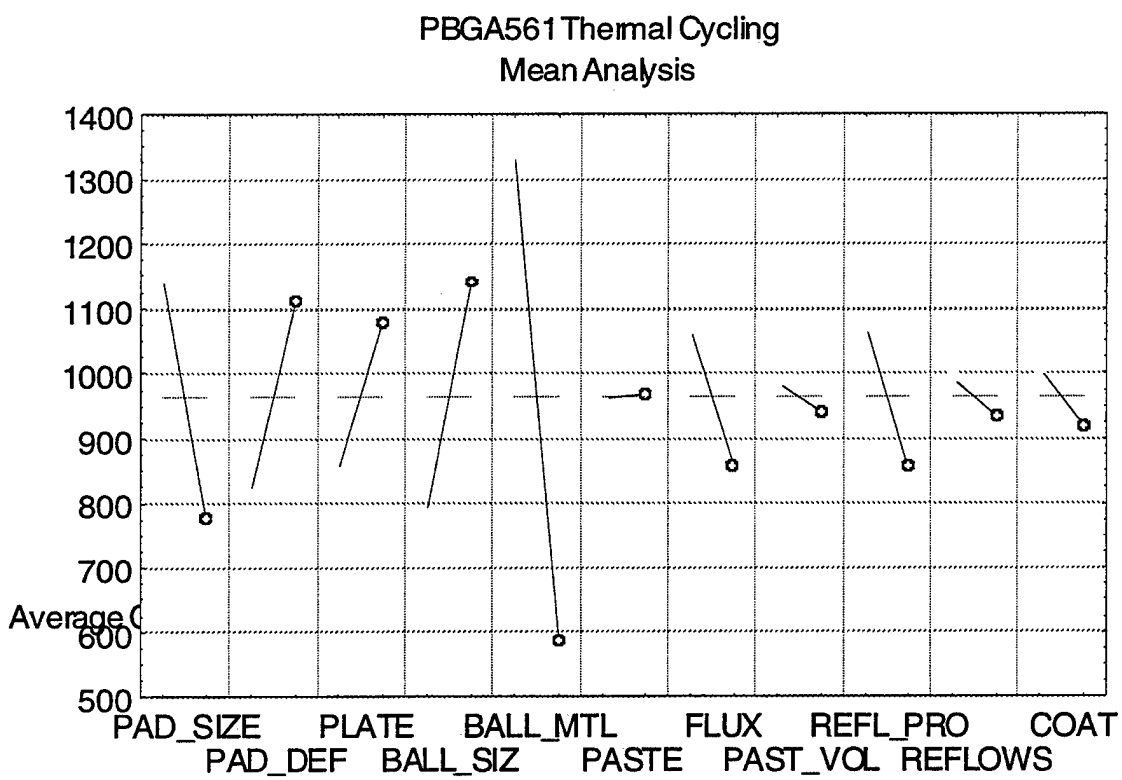


Figure 4.2.3.2.6.4-1PBGA561 Thermal Testing Means Analysis

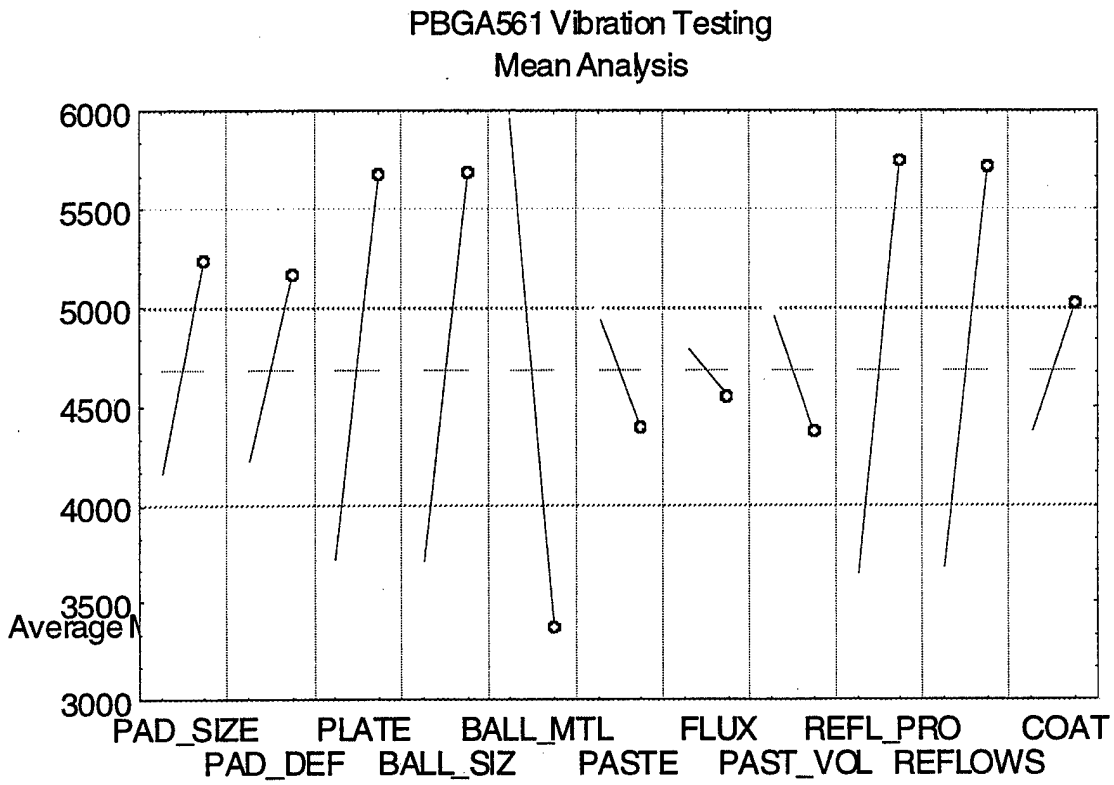


Figure 4.2.3.2.6.4-2 PBGA561 Vibration Testing Means Analysis

4.2.2.2.4.5 PBGA313

The PBGA313 packages all failed relatively early in the thermal cycling tests. Preliminary failure analysis shows that the failures invariably occur in the interface between the solder balls and the package substrate. This interface is often the site of large voids in the solder ball. These voids have been shown to be present in the as-received condition prior to assembly and reflow. Only 2 of the parts did not survive the full 6000 minutes of vibration.

The Response Table is shown in Table 4.2.3.2.6.5-1. The Factor Analysis for PBGA313 thermal cycling is shown in Figure 4.2.3.2.6.5-1. There is insufficient data to generate a meaningful factor analysis graph for vibration.

Table 4.2.3.2.6.5-1 PBGA313 Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	320	233	452	303	810	Intact
2	71	123	39	123	Intact	Intact
3	108	126	124	154	Intact	Intact
4	163	177	123	165	Intact	Intact
5	149	146	126	199	Intact	Intact
6	178	197	155	205	Intact	Intact
7	160	163	137	156	Intact	Intact
8	125	125	125	113	2564	Intact
9	231	231	241	251	Intact	Intact
10	364	452	384	410	Intact	Intact
11	364	279	72	145	Intact	Intact
12	121	90	112	90	Intact	Intact

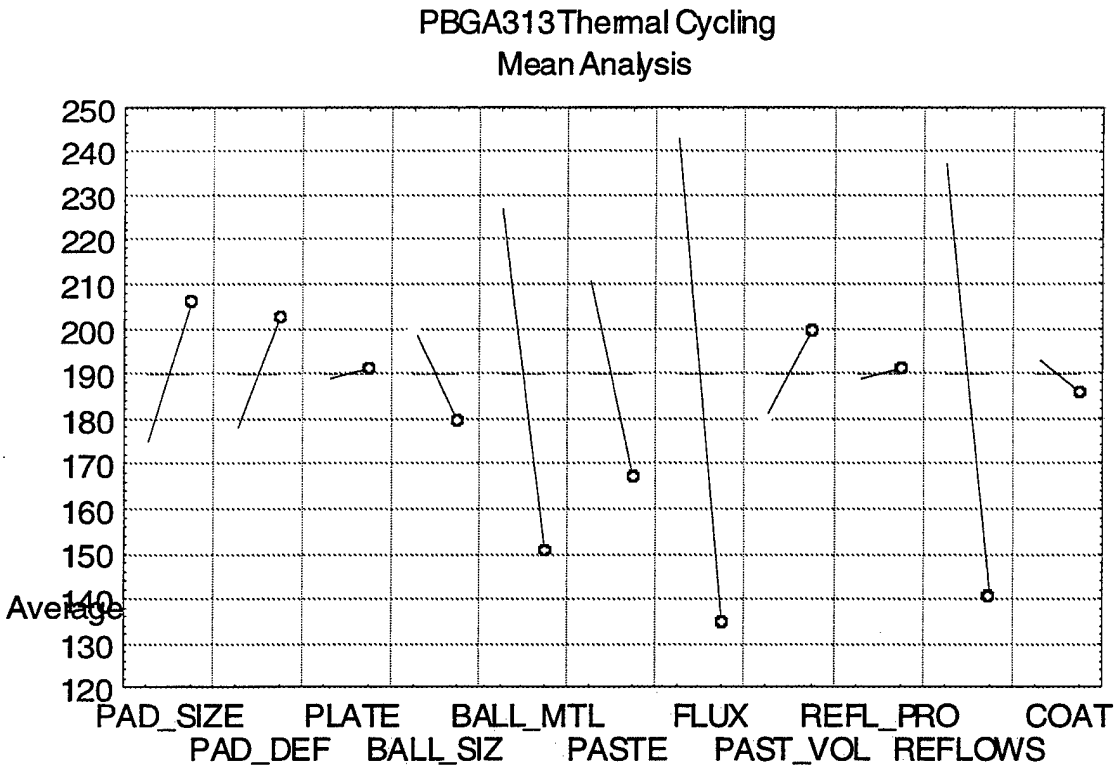


Figure 4.2.3.2.6.5-1 PBGA313 Thermal Cycling Means Analysis

4.2.2.2.4.6 PBGA169

Almost all of the PBGA169 packages had failed by the midpoint of thermal cycling test. Only 2 parts did not survive the full 6000 minutes of vibration.

The Response Table for the PBGA169 package is shown in Table 4.2.3.2.6.6-1. The Factor Analysis for PBGA169 thermal cycling is shown in Figure 4.2.3.2.6.6-1. There was insufficient data to generate a meaningful factor analysis graph for vibration testing.

Table 4.2.3.2.6.6-1 PBGA169 Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	364	233	747	452	1470	Intact
2	264	71	364	124	Intact	Intact
3	325	124	342	124	Intact	Intact
4	202	163	236	125	Intact	Intact
5	254	149	254	126	1320	Intact
6	362	23	404	251	Intact	Intact
7	400	199	309	153	Intact	Intact
8	464	279	586	201	Intact	Intact
9	370	90	409	221	Intact	Intact
10	1126	594	833	833	Intact	Intact
11	453	615	1323	131	Intact	Intact
12	177	112	177	112	Intact	Intact

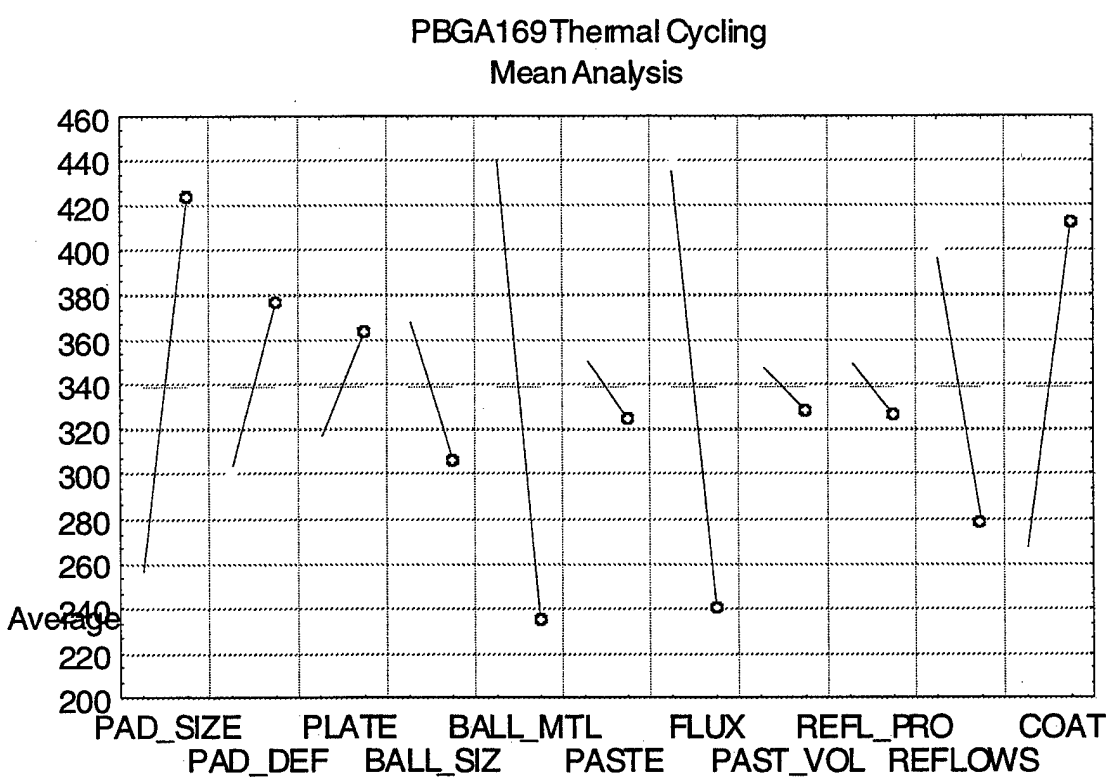


Figure 4.2.3.2.6.6-1 PBGA169 Thermal Cycling Mean Analysis

4.2.2.2.4.7 *Discrete Components*

The discrete packages included in the DOE 1 study were chosen because they were unique package styles for the AEN plant, or, as in the case of the CDR35 capacitors, were the most likely to fail, based on their materials and size. The discrete components each had their part terminations shorted and were chained together on the circuit board so the solder joints could be monitored in the same way as the multi-leaded packages.

All of the discrete parts survived the full 6000 minutes of vibration. Two of the CDR35 parts, the .180 X .250 inch ceramic chip capacitors, had cracked solder joints before the completion of the full 2000 thermal cycles. One part was from a circuit board with factor combination number 1 and the other was among the parts assembled with factor combination 12. These two parts had 3 factors in common: they used eutectic solder, received a smaller solder paste volume for their joints and had no conformal coat. The Response Table is shown in Table 4.2.3.2.6.7-1. There was insufficient data to generate a meaningful factor analysis graph.

Table 4.2.3.2.6.7-1 Discretes Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	Intact	Intact	1618	Intact	Intact	Intact
2	Intact	Intact	Intact	Intact	Intact	Intact
3	Intact	Intact	Intact	Intact	Intact	Intact
4	Intact	Intact	Intact	Intact	Intact	Intact
5	Intact	Intact	Intact	Intact	Intact	Intact
6	Intact	Intact	Intact	Intact	Intact	Intact
7	Intact	Intact	Intact	Intact	Intact	Intact
8	Intact	Intact	Intact	Intact	Intact	Intact
9	Intact	Intact	Intact	Intact	Intact	Intact
10	Intact	Intact	Intact	Intact	Intact	Intact
11	Intact	Intact	Intact	Intact	Intact	Intact
12	Intact	Intact	1908	Intact	Intact	Intact

4.2.2.2.4.8 *CBGA561*

Because of the size of this package, and the large mismatch in CTE between the part and the cored circuit board module, the CBGA561 packages were not expected to last many thermal cycles. Most of the CBGA561 parts, however, had a discontinuity before they even entered the test.

Further testing showed that failures were occurring during preliminary adhesive cure stages, and that the failure mode was the separation of the ball attach pad from ceramic BGA substrate, rather than failure of the solder joint itself.

Cure temperatures for the circuit boards subjected to vibration testing were lowered to reduce the incidence of premature failure. Still, most of the parts subjected to vibration failed early in the vibration test.

The Response Table is shown in Table 4.2.3.2.6.8-1. The Factor Analysis for CBGA561 thermal cycling is not shown. The Factor Analysis for CBGA561 vibration cycling is shown in Figure 4.2.3.2.6.8-1.

Table 4.2.3.2.6.8-1 CBGA561 Response Table

	Thermal Cycles to Failure				Vibration Miinutes	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	0	0	0	0	1260	840
2	0	0	0	0	60	60
3	5	5	5	1	120	157
4	5	5	0	5	720	121
5	0	0	5	0	465	704
6	0	0	0	0	421	613
7	0	0	0	0	60	60
8	5	5	0	5	133	156
9	0	0	0	0	360	360
10	0	0	0	0	445	360
11	0	0	0	0	360	1440
12	0	10	0	0	360	1465

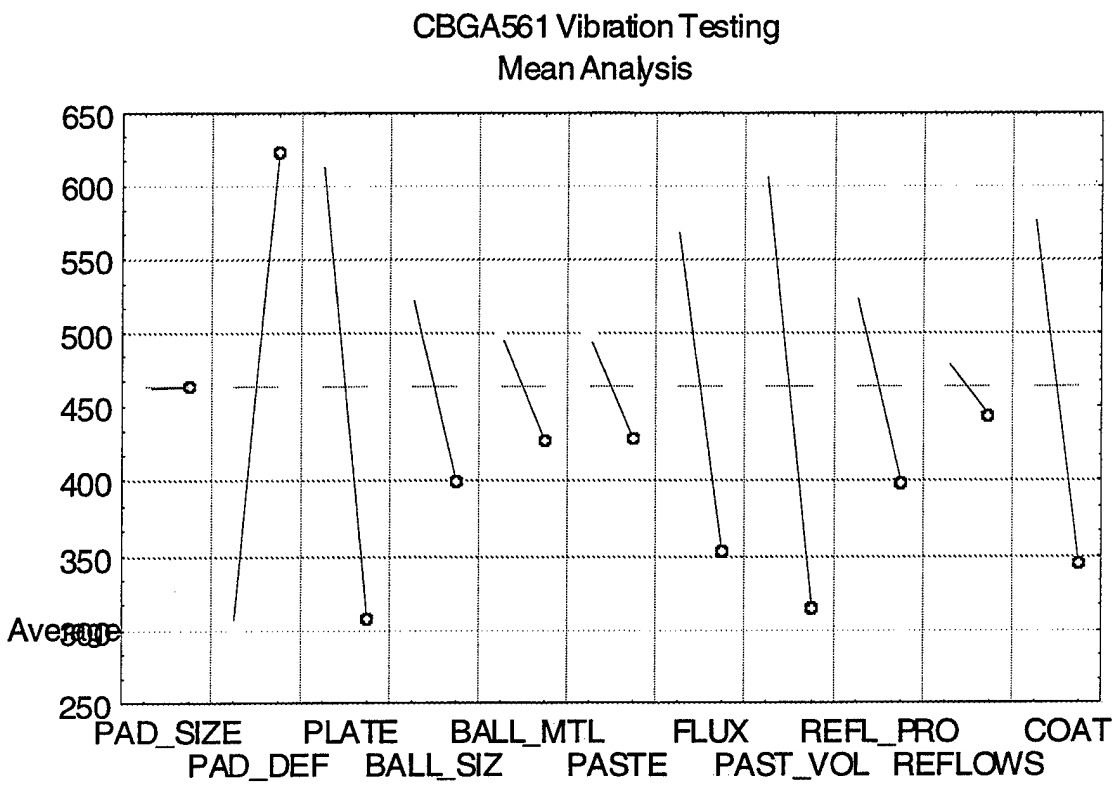


Figure 4.2.3.2.6.8-1 CBGA561 Vibration Testing Mean Analysis

4.2.2.2.4.9 CBGA625

The CBGA625 packages also had a large number of early failures for both thermal cycling and vibration. Again, it is likely that preliminary adhesive cures caused failures in the thermal cycle modules prior to the start of the thermal cycling test.

The Response Table is shown in Table 4.2.3.2.6.9-1. The Factor Analysis for CBGA625 thermal cycling is shown if Figure 4.2.3.2.6.9-1, although it is doubtful how significant the data is. The Factor Analysis for CBGA561 vibration cycling is shown in Figure 4.2.3.2.6.9-2.

Table 4.2.3.2.6.9-1 CBGA625 Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	17	10	5	0	720	Intact
2	5	0	0	0	60	60
3	0	0	5	5	126	180
4	5	5	5	0	60	2880
5	0	0	1	0	60	62
6	5	0	0	0	60	360
7	5	10	0	5	60	Intact
8	0	5	5	13	115	720
9	5	0	5	0	360	360
10	5	5	13	5	471	1440
11	0	1	0	0	720	360
12	0	0	5	0	46	1440

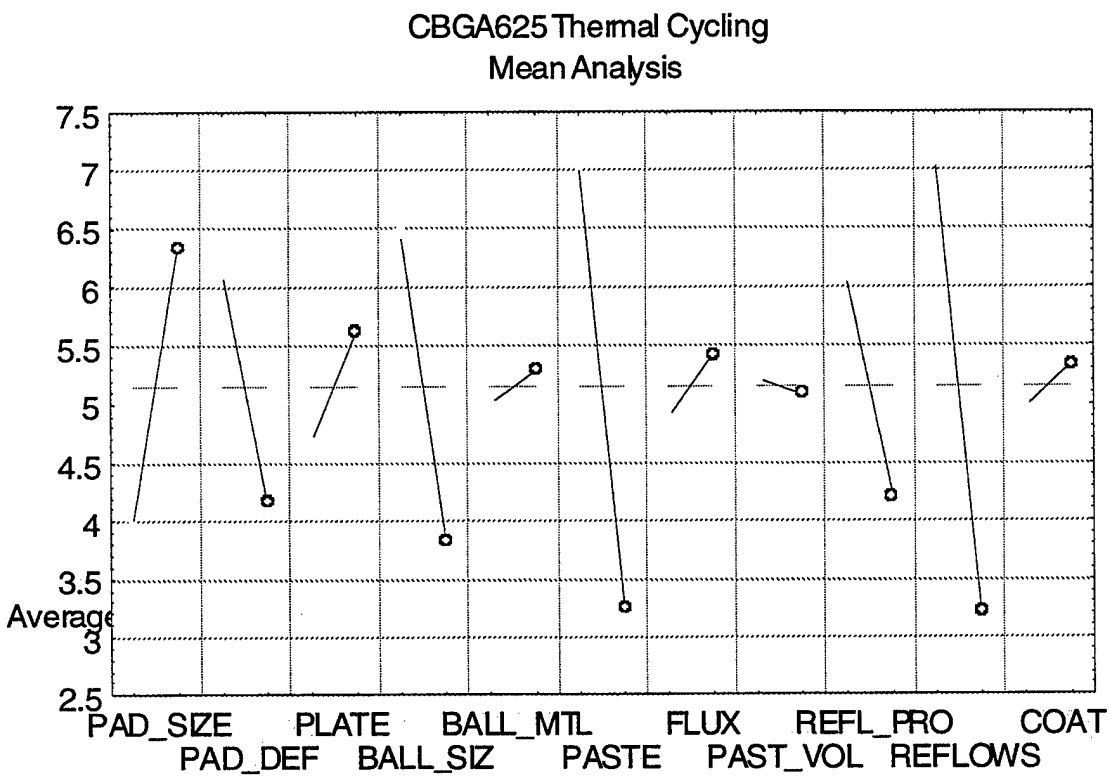


Figure 4.2.3.2.6.9-1 CBGA625 Thermal Cycling Means Analysis

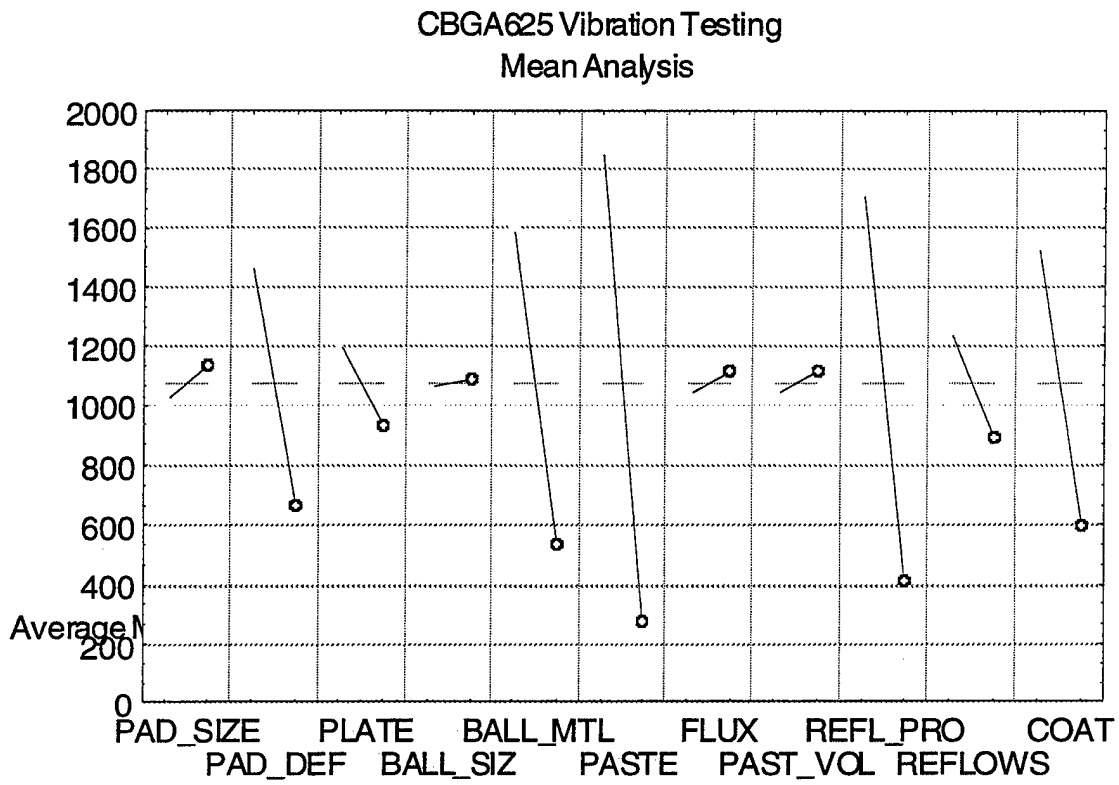


Figure 4.2.3.2.6.9-2 CBGA625 Vibration Testing Means Analysis

4.2.2.2.4.10 CBGA256

Most of CBGA256 packages made it into thermal cycling without premature failures from elevated adhesive cure temperatures. Although there were some early failures in vibration, a good portion of the parts survived the full 6000 minutes of vibration. All of the parts that survived were located towards the edge of the board, where they would see less deflection during vibration.

The Response Table is shown in Table 4.2.3.2.6.10-1. The Factor Analysis for CBGA256 thermal cycling is shown in Figure 4.2.3.2.6.10-1. The Factor Analysis for CBGA256 vibration cycling is shown in Figure 4.2.3.2.6.10-2.

Table 4.2.3.2.6.10-1 CBGA256 Response Table

	Thermal Cycles to Failure				Vibe Minutes to Failure	
	Maximum Coplanarity		Minimal Coplanarity		Nominal Coplanarity	
	Center Part	Edge Part	Center Part	Edge Part	Center Part	Edge Part
1	5	17	0	17	810	Intact
2	5	5	5	1	720	134
3	5	18	13	13	159	1856
4	13	5	18	13	363	1800
5	0	0	10	5	649	Intact
6	17	10	17	10	60	Intact
7	17	17	22	22	507	Intact
8	23	64	29	13	1400	4920
9	17	10	10	10	1440	Intact
10	5	18	13	23	1860	Intact
11	1	1	5	5	366	360
12	17	22	17	17	1465	Intact

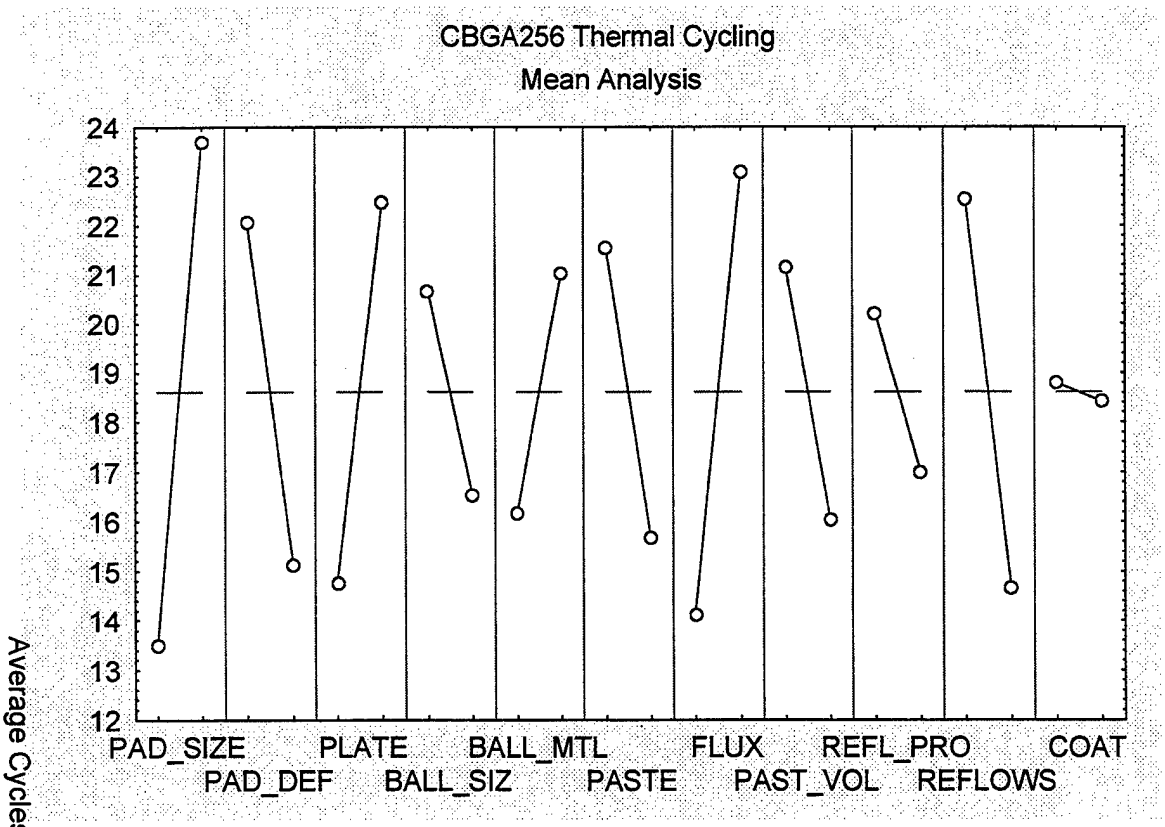


Figure 4.2.3.2.6.10-1 CBGA256 Thermal Cycling Means Analysis

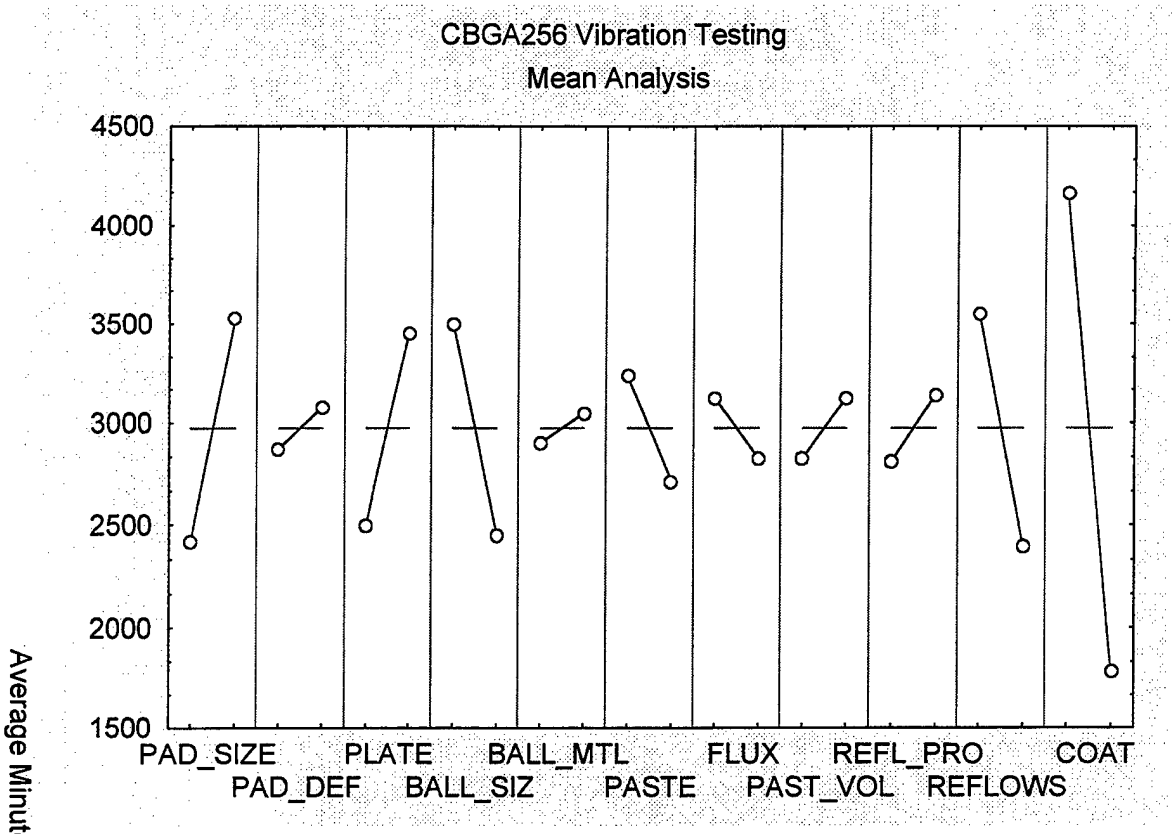


Figure 4.2.3.2.6.10-2 CBGA256 Vibration Testing Means Analysis

4.2.2.2.4.11 QFP240

All of the QFP240 joints survived vibration and thermal cycling. There were problems, however, with bridging of adjacent leads when printed with the 8 mil thick stencils.

4.2.2.2.5 DOE 1 Test Results by Control Factor

A summary of the Means Analysis graphs is tabulated in Table 4.2.2.2.7.11-1. Effects are categorized as a major effect if it added 25% to the average life. Minor effects added between 15% and 25% to the average life. Any factor that added less than 15% to the average solder joint life was considered insignificant in the face of experimental noise.

4.2.2.2.5.1 Pad Size

There was a preference for smaller pad sizes among the ceramic parts and the PBGA169, however, the life of the PBGA561 showed a minor improvement with larger pads.

4.2.2.2.5.2 Pad Definition.

Both the ceramic and the plastic BGA561 packages showed a preference for pads that were not solder mask defined, however the smaller ceramic BGAs showed better durability with pad defined by solder mask.

4.2.2.2.5.3 Pad Plating

Two BGA package styles had minor positive effects when mounted on Enthone-coated copper pads, but the CBGA561 showed a major positive effect when mounted on the normal solder plated pads. However, there were some instances of Enthone-coated boards having opens that were most likely caused by unsolderable pads.

4.2.2.2.5.4 Ball Size

The PBGA561 had minor positive effects for both thermal cycling and vibration testing when built with larger solder balls. Other parts showed effects for small balls. However, only the plastic and ceramic BGA561 parts were built with 2 different sizes of solder balls.

4.2.2.2.5.5 Ball Material

Only the ceramic and plastic BGA561 packages had varying ball types. The PBGA 561 showed major durability improvement when using the eutectic solder balls instead of the balls that did not reflow during soldering. Some of the BGAs that did not have varying ball materials showed significant durabilty increases when the BGA561 parts on that board had the eutectic balls. This may be due either a factor interaction in the L12 array or an unknown physical effect on the circuit boards.

4.2.2.2.5.6 Solder Paste

Both the TSOP32 and the CLCC32 packages showed major increases in durability with the Indium solder paste. The smaller ceramic BGAs had durability increases with the Sn63Pb37 eutectic solder paste.

4.2.2.2.5.7 Flux Type

The more active flux types showed up as significant effects for several package styles, however, the CBGA256 showed a major improvement when soldered with no clean flux.

4.2.2.2.5.8 Solder Paste Volume

Solder paste volume was not generally a significant factor, although it did show up as a major improvement when more paste was used for the CBGA561 package.

4.2.2.2.5.9 Reflow Profile

Most package styles did not have a significant response to reflow profile. The CBGA625 showed improved durability with the slower profile, while the PBGA561 had minor improvement under vibration with the nominal profile.

4.2.2.2.5.10 Second Reflow

There was a trend towards the second, inverted reflow pass improving thermal cycling solder joint durability for BGAs. The cause of this was initially thought to be an increase in standoff height improving the geometry of the solder joints, but measurements showed the BGA standoffs do not increase significantly when inverted during reflow. Further analysis will focus on positioning of voids in the BGA balls.

4.2.2.2.5.11 Conformal Coat

The addition of a silicone conformal coat had a negative effect on the ceramic BGAs, particularly for vibration testing. It had no effect on the majority of the rest of the parts, except for adding some durability to the PBGA169 and CLCC32.

4.2.2.2.5.12 DOE 1 Paper Champion

The paper champion of the DOE 1 test is the design concept that incorporates the best attributes of each control factor in the presence of the noise factors. The DOE 1 test array was orthogonal, so the paper champion represents a condition that is not tested in the array but should produce the best results. Factors that had insignificant effect on cycles to life, or that had opposite effects on different part styles were selected by manufacturing to optimize producibility.

The plastic component paper champion included:

- Large solder pads, preferred by manufacturing, mixed test results
- Non solder mask defined pads, benefit to large PBGAs and CBGAs in thermal cycling
- Solder pad plating, preferred by manufacturing, mixed results
- Ball size as supplied, mixed results, preferred by suppliers

- Ball material Sn 62, best results, preferred by the suppliers
- Paste material Sn 63, less expensive, no impact on PBGAs, preferred by manufacturing
- Flux active, strong influence on cycles to failure, no significant cost impact
- Paste volume high, easily achieved with large pads and non solder mask defined pads
- Reflow profile nominal, moderate impact, preferred by manufacturing
- Reflow passes, twice, strong impact but disliked by manufacturing. Adequacy of single pass re-evaluated at DOE2
- Conformal coat silicone, moderate improvement over no coat, basic planned manufacturing process.

Table 4.2.2.2.7.11-1 shows the summary of the means analysis for all the parameters that were examined as part of the DOE 1 test.

Table 4.2.2.2.7.11-1 Summary of Means Analysis

PART	TEST	PAD SIZE	PAD DEFINE	PAD PLATE	BALL SIZE	BALL MATL	PASTE MATL	FLUX	PASTE VOLUME	REFLOW PROFILE	REFLOW PASSES	CONF COAT
TSOP32	THERM VIBE						INDIUM	active				
JLEAD32	THERM VIBE											
CLCC32	THERM VIBE	small	define		small		INDIUM					silicone
PBGA561	THERM VIBE	large	clear	copper	large large	SN62 SN62				nominal	once	
PBGA313	THERM VIBE					sn62		ACTIVE			TWICE	
PBGA169	THERM VIBE	small				SN62		ACTIVE			twice	silicone
DISCRETES	THERM VIBE											
CBGA561	THERM VIBE		CLEAR	SOLDER				active	MORE			none
CBGA625	THERM VIBE	small	define DEFINE		SMALL	SN62	SN63 SN63			slow SLOW	TWICE	NONE
CBGA256	THERM VIBE	SMALL small	define	copper copper	SMALL small		SN63	NOCLN			twice twice	none NONE

ALL CAPITALS = MAJOR EFFECT (ADDS >25% TO LIFE)
Small letters = minor effect (adds 15-25% to life)
Empty cells = insignificant or unmeasurable effects

Lightly shaded areas denote factors not applicable to that part style.

4.2.2.2.6 DOE 2 Experimental Design

The primary purpose of this experiment is to define design parameters that result in BGA solder joints that meet the required durability. This DOE used an L4 orthogonal Array to determine effects of some design parameters coupled with various board core combinations to parametrically determine the effect of different CTEs and natural frequencies. Parameters and levels were chosen that have primary contribution to strain of BGA solder joints.

Each Module consisted of two boards with four BGAs of each size (352, 313, 256, 225, 169). The four BGAs have parameters varied to make-up the L4 array for each module. The factors that were studied for the array are:

- Underfill/Coating Material
- Part Bake Out Cycle
- Stand-off

Board design and process parameters were per the "paper champion" of DOE #1. The IBM parts were mechanically similar to the DV parts. For the LSI parts, no mechanically representative parts were available so "dummy" stitched Topline parts were used. The L4 array is shown in Table 4.2.2.2.8-1.

Table 4.2.2.2.8-1 DOE 2 L4 Orthogonal Array

Parameter>	Underfill/Coating	Bake Out Cycle	Standoff
L1	Material 1	Long	Yes
L2	Material 1	Short	No
L3	Material 2	Long	No
L4	Material 2	Short	Yes

BGA Underfill / Coating

This factor was used to study the effect on joint life of different underfill materials. TRW AEN considered two silicone materials, Dow Corning DC 1-2577 Low VOC and HumiSeal 1C55, viable. The HumiSeal 1C55 is compatible with the topcoat of DC 1-2577 used for conformal coat.

The factor was perceived to have both a positive impact on life by adding mechanical strength and dampening to the component attach and a negative impact at cold temperatures as the material could become rigid and act to add tensile load to the solder joints.

Component Bake Out Cycle

The method of procurement of the IBP-MPCL components differed from the TRW AEN "norm" due to low volumes of acquisition. Moisture sensitive part control was often unknown. All components were baked prior to assembly to remove accumulated moisture. Repetitive builds caused repetitive baking of the same reel of components. Oxide formation and reduced solderability (and joint life) were a concern.

The levels set for this factor were 24 hours at 100°C and 168 hours at 50°C.

BGA Stand Off

Lengthening the solder joint (increasing distance from the component to the circuit card), distributes the shear stress on the joint over a longer column. This should improve cycles to failure. This factor was studied by installing chip components under the perimeter of the BGAs. During solder reflow, the chip component mechanically limited the collapse of the BGA solder sphere. Presence and absence off the chips were the selected levels.

The vibration and thermal cycling environments used for this experiment are the same as those used for DOE 1. For vibration testing, the board core combinations are chosen to parametrically vary the natural frequency. The combinations chosen are:

- BT Epoxy Board soft bonded to P120 Core
- BT Epoxy Board soft bonded to Al Core
- BT Epoxy Board soft bonded to BeBeO Core
- BT Epoxy Board hard bonded to BeBeO Core

For thermal cycling tests, the board and core combinations were chosen to parametrically vary the CTE. The Duroid boards were chosen because of their low elastic modulus. Each combination is repeated at least twice to increase the fidelity of the data. The combinations chosen are:

- BT Epoxy Board soft bonded to P120 Core
- BT Epoxy Board soft bonded to an Aluminum Core
- BT Epoxy Board soft bonded to an Al/C-C Core
- Thermount Board soft bonded to P120 Core
- Duroid Board soft bonded to P120 Core
- Duroid Board hard bonded to P120 Core

Table 4.2.2.2.8-2 shows the predicted variation in CTE and natural frequencies for the test combinations chosen.

Table 4.2.2.2.8-2 DOE 2 Predicted CTE and Natural Frequency

Board/Bond/Core Combination	CTE	Fn
BT-Soft-P120	16 ppm/°C	500 Hz
BT-Soft-Al	18 ppm/°C	400 Hz
BT-Soft-BeBeO	Vibe only	550 Hz
BT-Hard-BeBeO	Vibe only	900 Hz
BT-Soft-Al/C-C	16 ppm/°C	650 Hz
Kev-Soft-P120	13 ppm/°C	Thermal Cycling Only
Duroid-Soft-P120	Low Modulus	Thermal Cycling Only
Duroid-Hard-P120	Low Modulus	Thermal Cycling Only

Figure 4.2.2.2.8-1 shows a picture of a DOE 2 module. As in DOE1, solder joints were chained together and connected to test equipment that monitored each circuit for discontinuities.

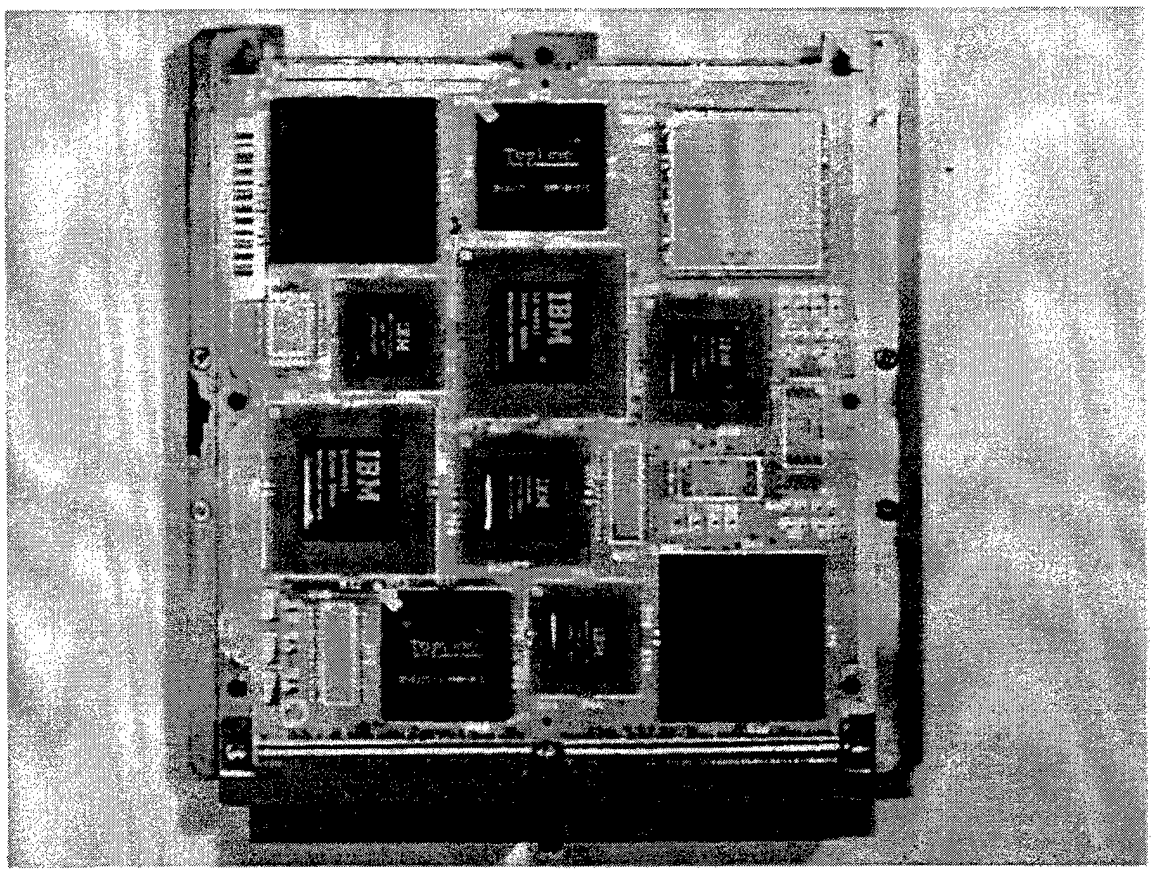


Figure 4.2.2.2.8-1 DOE 2 Module Layout

4.2.2.2.7 DOE 2 Thermal Cycling Test Results

Larger packages are expected to fail before the smaller ones, given that CTE mismatch is the primary driver to solder joint failures. In this case, the glob top packages built by IBM out-lasted the plastic over-molded packages available from Topline. This suggests either a difference in composite CTE between the two packaging technologies, or process variations. The Topline packages had solder joints that had a great deal of voiding in them, prior to placement and reflow. Studies have suggested that when voids exceed 15% of the cross-sectional area of a solder joint, the fatigue life of the joint begins to decrease.

Taken as a group, the packages performed best when mounted on BT Epoxy boards soft-bonded to the composite materials, P120 and Aluminum-Carbon-Carbon. The BT epoxy boards also performed well when bonded to Aluminum.

The soft-bonded Thermount boards had the least amount of variance between packaging sizes and technologies. This suggests a shift in failure mode.

The data for the soft-bonded Duroid boards show the widest variation in cycles to failure. The hard-bonded Duroid boards had the earliest average cycles to failure.

The BT epoxy / soft bond combination is the preferred design solution. The preceding data includes all effects due to the 3 factors studied as a design of experiments. Design of Experiments means analysis extracts the effects of each factor on the average cycles to first failure. The results are shown in Figure 4.2.2.2.8-2. The average increase in life is only in the 2-3% range. Given the small sample sizes, these increases are not significant.

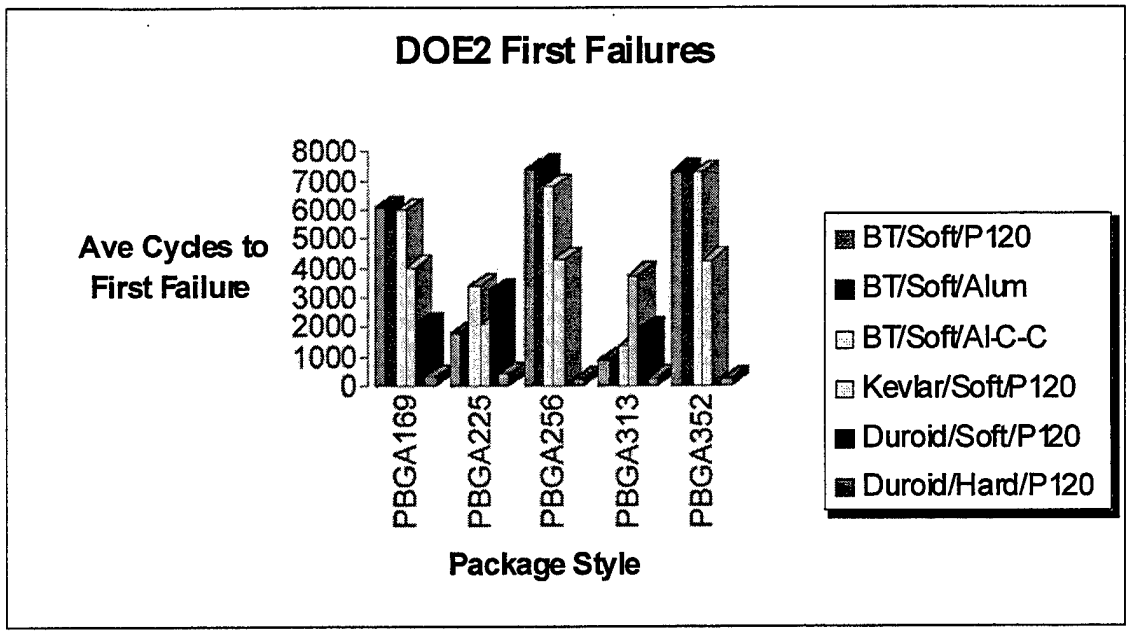
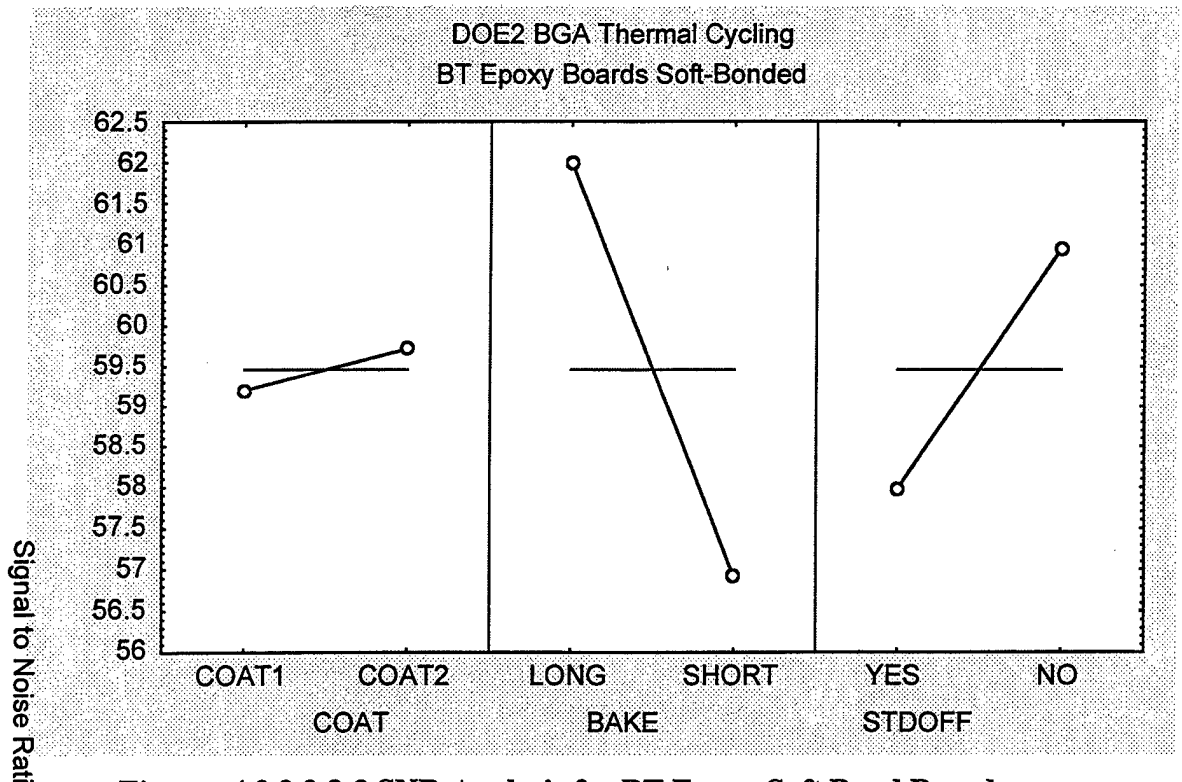


Figure 4.2.2.8-2 First Failure Summary by Part Type

The SNR can be calculated for each factor. The signal-to-noise ratio shows which factors most reduce the variability of the number of cycles to failure. Figure 4.2.2.2.8-3 shows the signal to noise ratio analysis. The long bake cycle appears to reduce variability, along with having no standoffs. Figures 4.2.2.2.8-4 through 4.2.2.2.8-9 show the means analysis for the individual parts.



Figures 4.2.2.2.8-3 SNR Analysis for BT Epoxy Soft Bond Boards

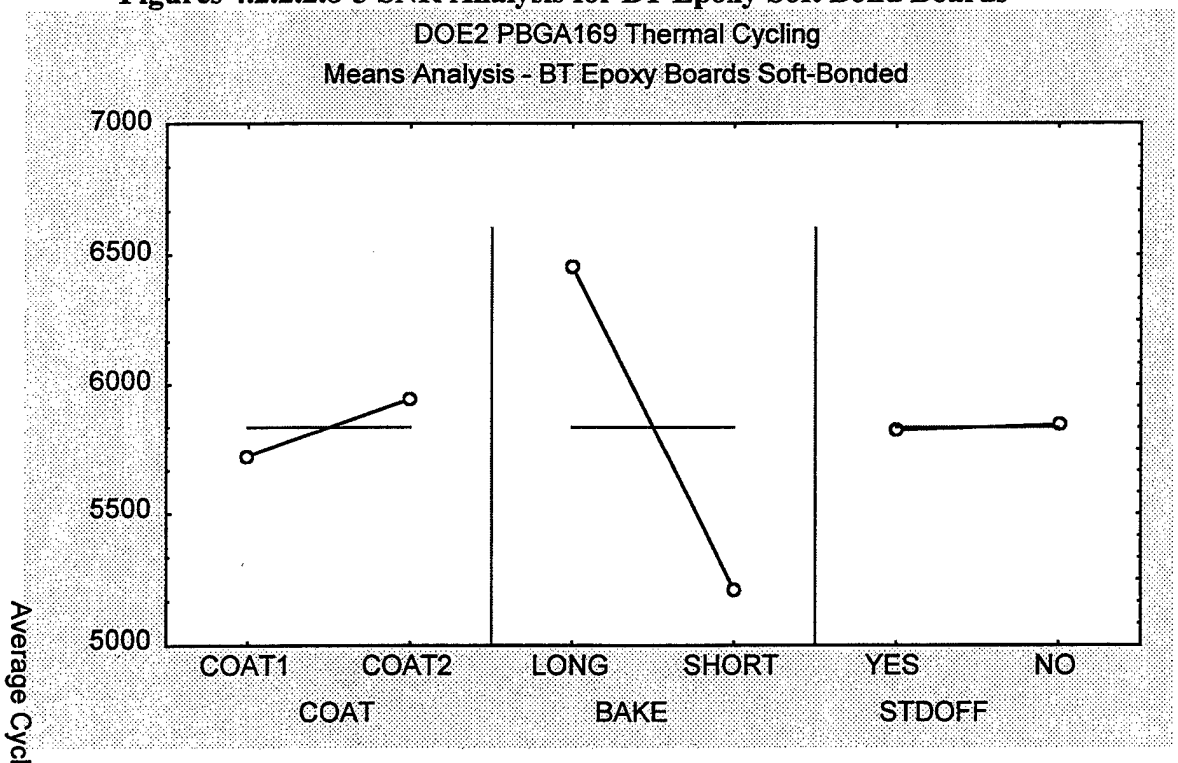


Figure 4.2.2.2.8-4 Results of 23 mm package

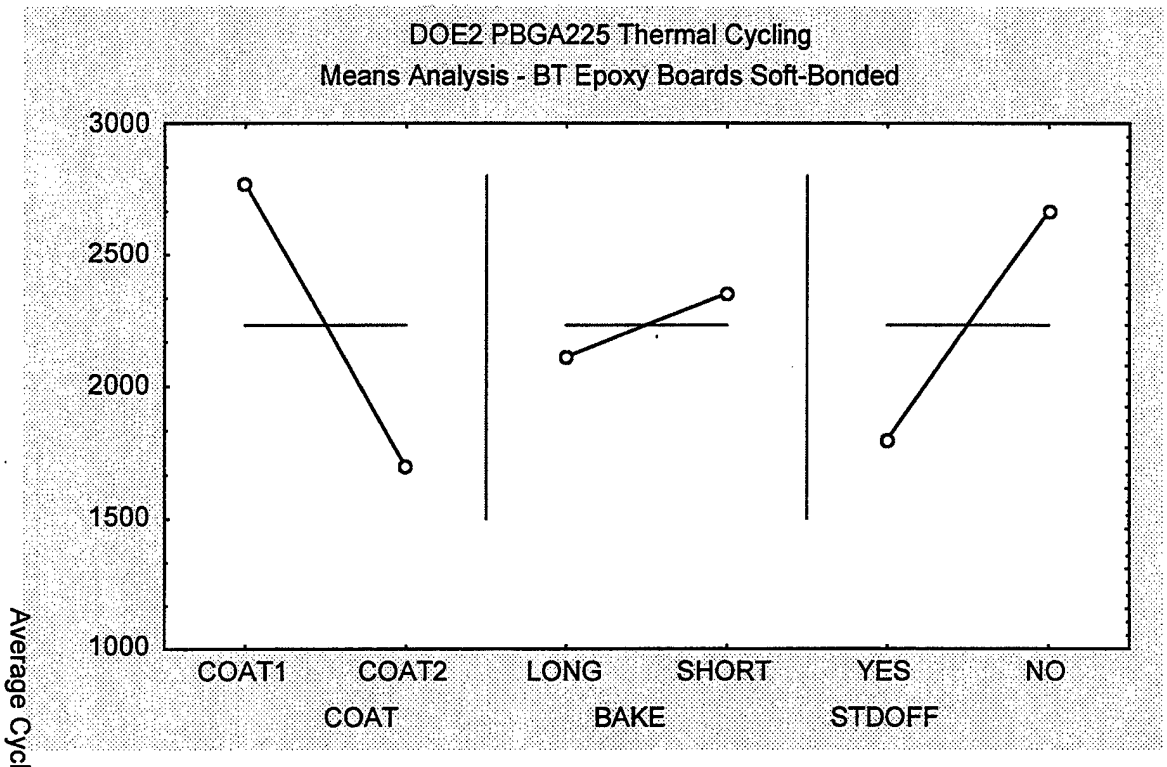


Figure 4.2.2.2.8-5 Results of PBGA 225 Package

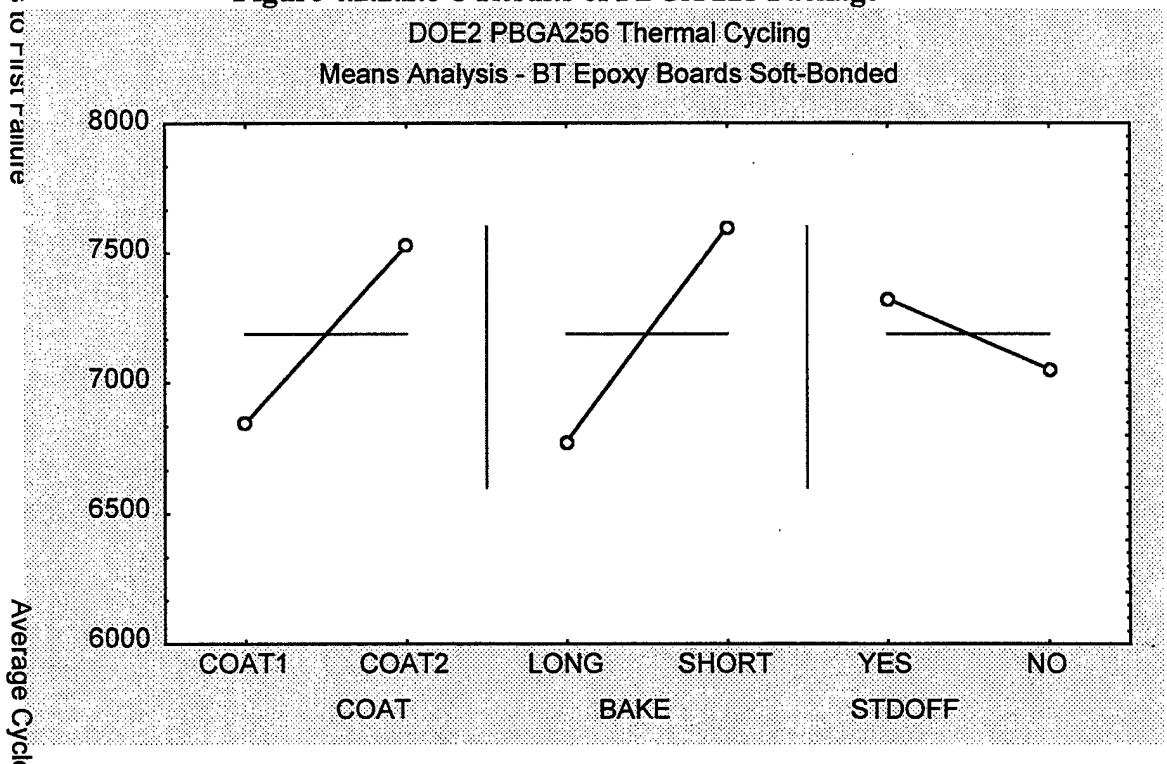


Figure 4.2.2.2.8-6 Results of PBGA 256 Package

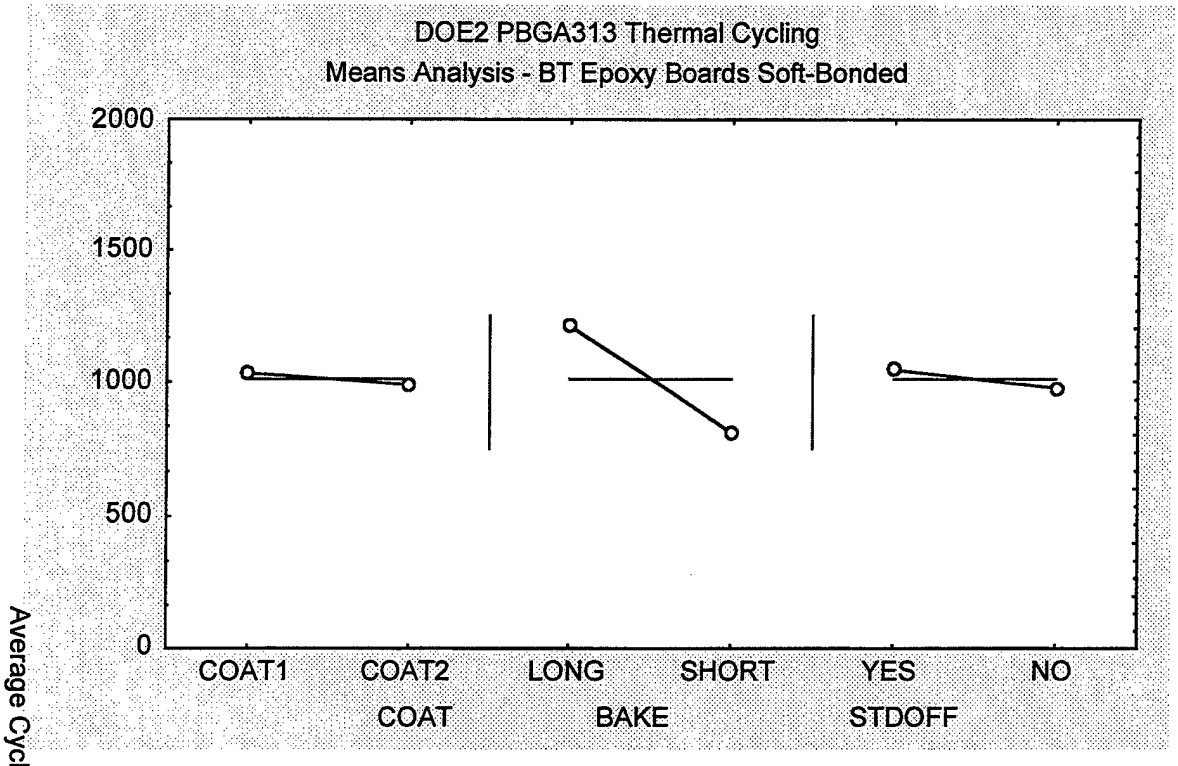


Figure 4.2.2.2.8-7 Results of PBGA 313 Package

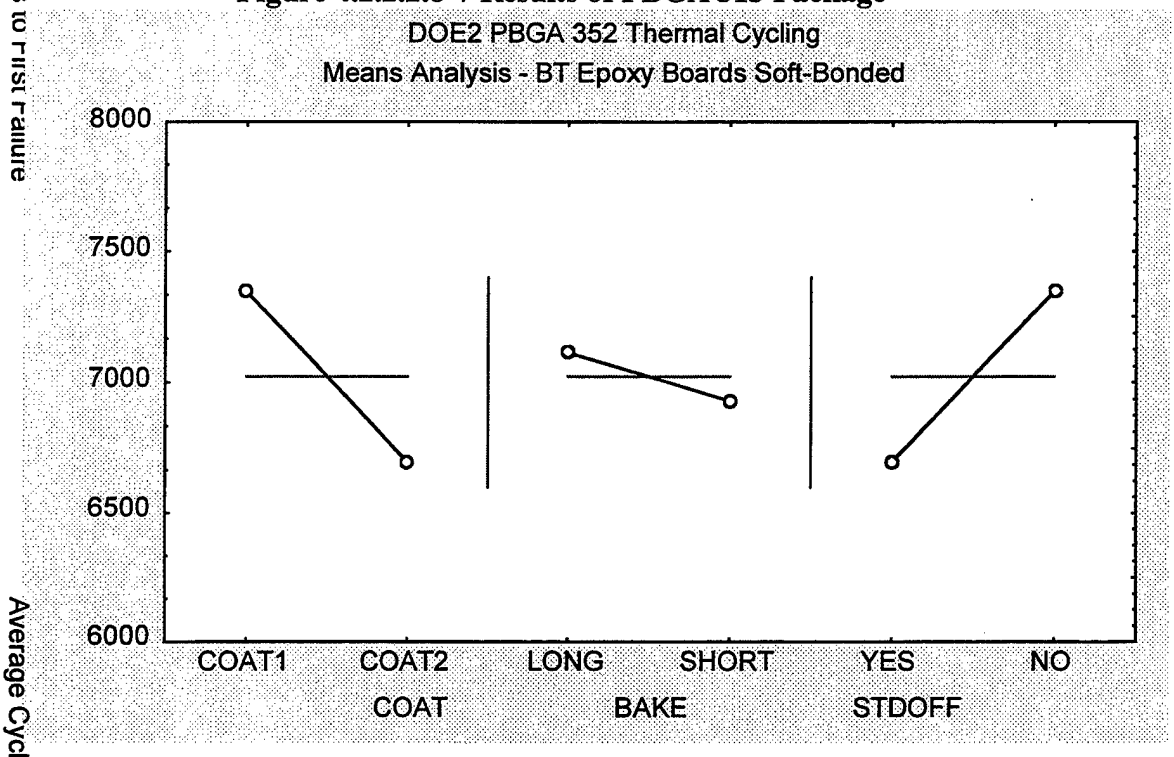


Figure 4.2.2.2.8-8 Results of PBGA 352 Package

BGA Underfill / Coating

Modules with no conformal coat were used as a control in addition to the orthogonal (L4) array.

This also allowed for correlation between DOE 1 and DOE 2 findings. All modules with underfill and conformal coat performed better than those without. There were mixed results on the life effects of the Dow Corning DC 1-2577 Low VOC and HumiSeal 1C55 underfill. Some part types performed better with the Dow material. Other part types performed better with the HumiSeal. Selection of the underfill and coating types were left to manufacturing.

Component Bake-Out Cycle

The long duration bake out increased solder joint life for most part types and board to core combinations. The long bake also decreased the variance in solder joint life. From these test results, the longer bake cycle should be adopted.

Oxide and intermetallic formation reducing solderability are significant concerns to manufacturing. Components included in this DOE examination were closely controlled from receipt to use, and will not match those used in production. The protracted bake cycle is difficult and expensive to implement in the commercial manufacturing line. To satisfy these concerns, short bake cycles were selected for production.

BGA Stand Off

Absence of the BGA standoff increased the solder joint life for most part types and board to core combinations. From these results, no stand off should be used.

Lengthening the solder joint (increasing distance from the component to the circuit card), distributes the shear stress on the joint over a longer column, improving cycles to failure. The stand off used did not achieve this goal. The stand offs were positioned mid span on each side of the BGA, and may have caused uneven stand off and non-uniform stress distribution. Selection of ceramic chip stand offs may have caused increased tensile joint loading at cold extremes. Stand offs were not used for production.

4.2.2.2.8 DOE 2 Vibration Test Results

Vibration testing was performed on 6 different modules with varying natural frequencies as described in Section 4.2.2.2.7. Testing was performed for between 300 and 575 hours on these modules. The original plan of testing to the levels of DOE1 resulted in no significant accumulation of failures on the

modules. Vibration levels were stepped incrementally in order to determine fragility limits. Testing continued until the levels were up to $1g^2/Hz$. At this level there were still very few failures accumulated, especially on the stiffer module designs. Testing was suspended due to resource limitations. Failures that were recorded correlate with module stiffness. For the design environments and design solution, even the least stiff core tested (0.050 Aluminum) was sufficient to survive the design life.

4.3 Design Analysis

4.3.1 Reliability

4.3.1.1 IBP-MPCL Part Reliability Prediction

The reliability prediction methods used for the evaluation of components on the IBP-MPCL Program generally fall into the two basic categories: statistical/empirical methods and physics-of-failure methods. Information obtained from both methods has been used for the reliability evaluation of IBP-MPCL components.

4.3.1.1.1 Reliability Assessment Methods

The reliability evaluation of IBP-MPCL components was based on the following sources of information:

1. Part supplier qualification data
2. Part supplier reliability test monitor failure rate data
3. Part supplier conformance testing
4. Field use failure data (if and when available)
5. TRW CR1 and CR2 accelerated testing
6. Computer Aided Design of Microelectronic Packages (CADMP2)

CADMP2 can predict the time of occurrence for a specific failure mode in a specific device. Device life predictions with this tool are made based on the weakest link in the material or physical characteristics. Any variations in material properties or manufacturing defects are not accounted for with this tool.

4.3.1.1.2 CADMP2 Software Assessment Tool

The IBP-MPCL program used CADMP2 as a physics-of-failure reliability assessment tool. CADMP2 is not a stand-alone reliability prediction tool and as

such does not replace the need for reliability testing or field use data. It does not assess manufacturing defects or infant mortality defects. This is particularly important to keep in mind when performing an evaluation of a new, unproved package design. It has been used on IBP-MPCL for the following:

1. A guide for establishing the necessary accelerated test parameters for a given package/die geometry.
2. Determining the approximate expected life for a given set of conditions (i.e., using environment (avionics), package geometry/construction, die size, power dissipation, etc.).
3. Performing sensitivity analyses on a set of initial conditions (as described above in #2). In this case, key environmental parameters such as ambient temperature and humidity were varied and their effect on expected life was calculated.

Figures 4.3.1.1.2-1 through 4.3.1.1.2-3 are examples of the CADMP2 output data.

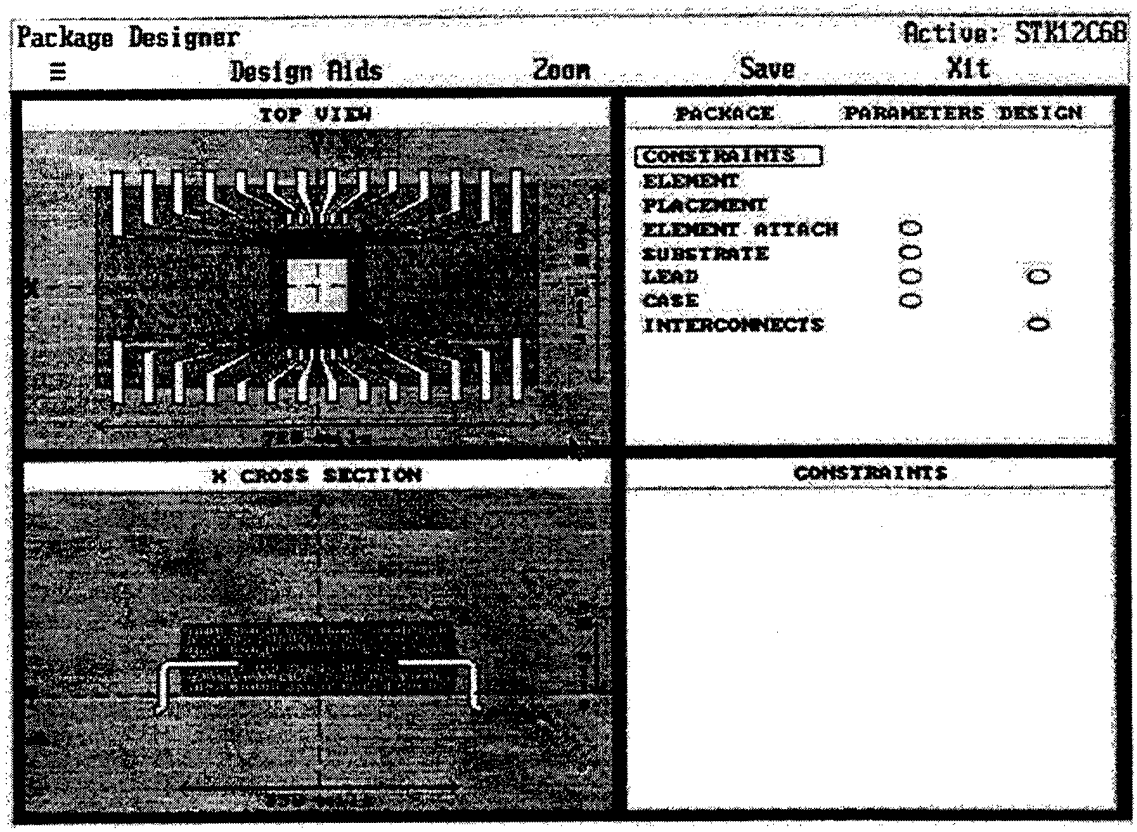


Figure 4.3.1.1.2-1 CADMP2 Input Screen for Device Package Parameters

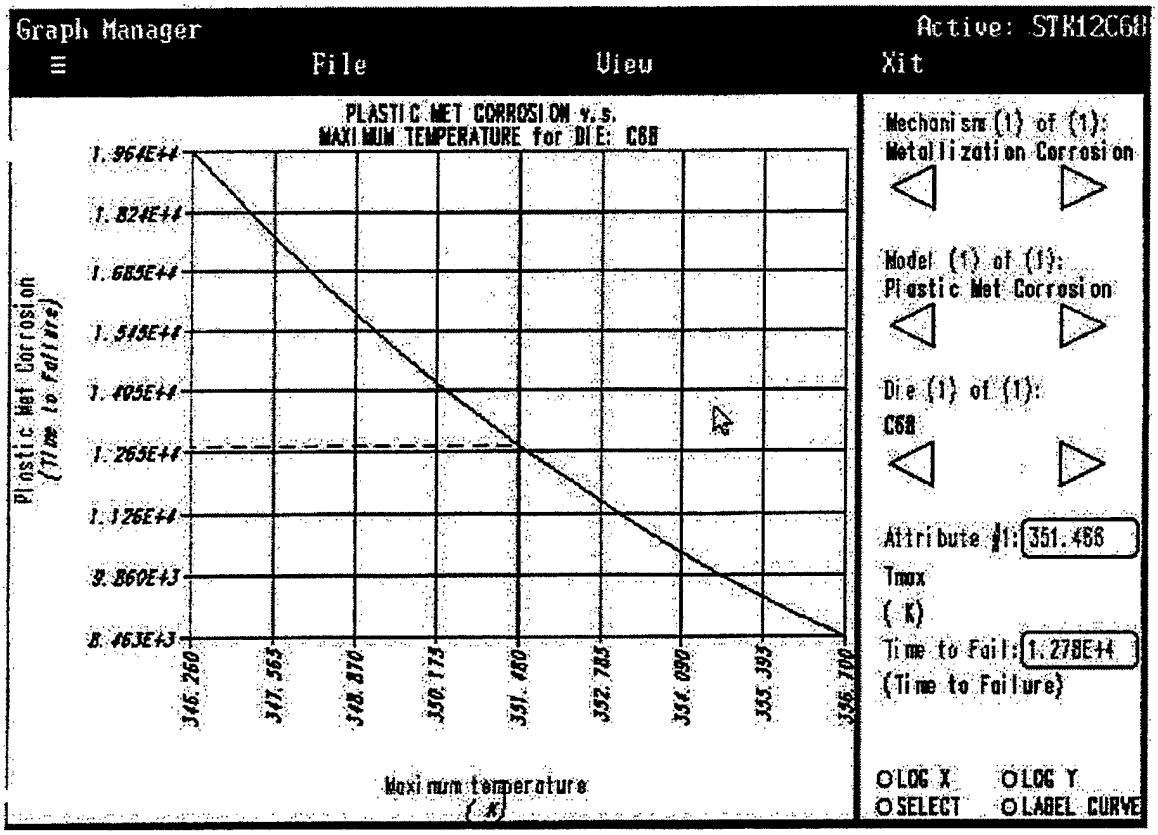


Figure 4.3.1.1.2-2 Graph for Corrosion Failure Mechanism (CADMP2)

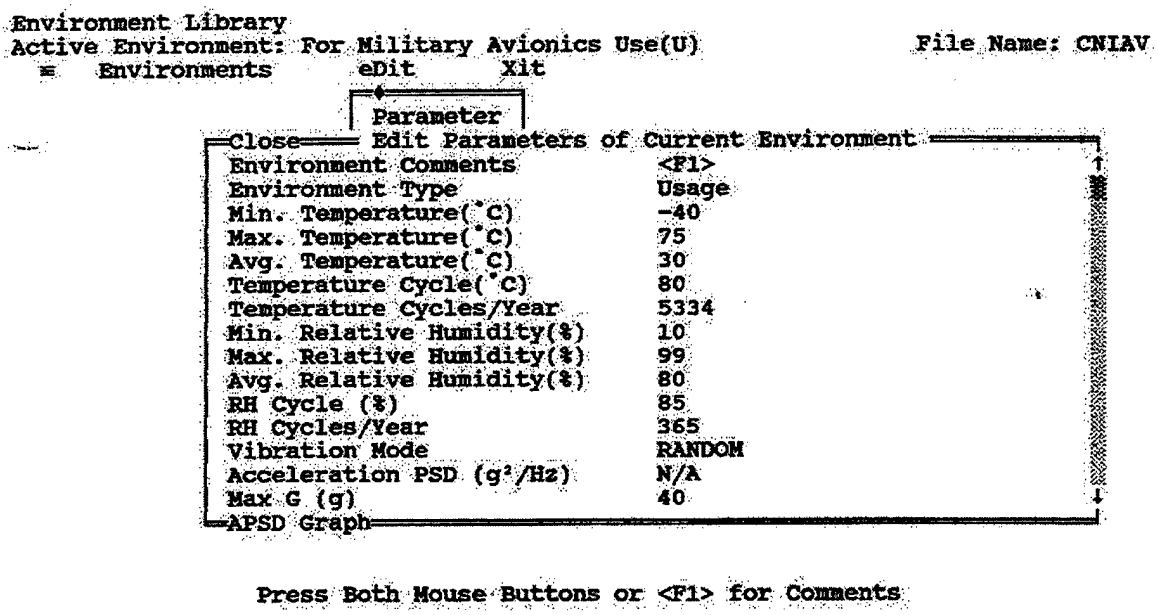


Figure 4.3.1.1.2-3 Device Environment Input Summary for CADMP2

4.3.1.2 Part Derating

The majority of the parts used on the IBP-MPCL program were either Military or Industrial temperature range parts. Some parts chosen for DV were only available in the commercial temperature range (0-70°C). This section documents the issues with these parts, the design margins associated with these parts, and the rationale for using them for the PV builds. These parts were the Motorola SRAM, IDT FIFO, IDT PLL, IDT Octal Bus Transceiver and the Cypress Prom.

The Cypress Prom (CY7C277-40JC) is a 32kx8, 40 nsec memory device. The commercial version of this part was ordered for the DV build. The derated setup and hold time margins calculated for this part were 1.4 and 1.25 nsec, respectively. This was considered to be inadequate, so a switch to the faster 30 nsec part was chosen for the PV builds. This provided an increase of 10 nsec timing margin. For the low quantity of parts purchased, an Industrial temperature version was determined to be cost prohibitive. Cypress parts were specified to have a –55 to +125C rating under electrical bias. They performed failure free during module level ESS on the Pre-PV test modules, and were used for production (PV).

The IDT FIFO (IDT72241L35J) is a 4kx9, 35 nsec, 0-70C part. The DV builds used the commercial temperature range part with no degradation in performance. For PV builds, an industrial temperature version (-40 to +85°C) was ordered by the part number IDT72241L35JI, as it was available with an insignificant cost premium.

The IDT Phase Lock Loop (PLL) 74FCT88915TT70 is not available in an industrial version. The leadless ceramic package versions that are available in military temperature range will not work with the design because of solder joint durability limitations. The IBP-MPCL design required that the part function at 20 MHz. The military part chosen was rated at 55 MHz. The IDT Applications Engineer stated that a commercial 70 MHz part can exceed the 55 MHz parts specifications at industrial temperatures. The faster 70 MHz part was chosen as a method of derating. These parts were installed on the CR2 component reliability test boards to verify performance. The critical specification to verify was the output to output skew measurement. One CR2 board (prior to life testing) was soaked for 20 minutes at +85°C and -40°C, then measured for skew. At -40°C, the worse case output to output skew was 470 psec. At room ambient the skew was 500 psec. At +85°C, the skew measured 540 psec. This results in a deviation of 40 psec. The maximum allowable skew from baseline design

documentation is 1000 psec. Twenty parts were measured after temperature cycling, autoclave, and HAST. These tests (which demonstrated several lifetimes on the parts) resulted in a worse case ambient skew of 560 psec at room ambient. With the maximum deviation of 40 psec over temperature, the derating is 39%. Concern existed over the conclusions drawn from the testing of one part at the temperature extremes. Five additional CR2 parts that were life tesed (as above) were tested over temperature. Clock to clock skew was measured at a maximum of 500 nsec at –40°C. The mean was 432 nsec and the standard deviation was 38 nsec. This indicated sufficient margin to use this part for PV.

The IDT Octal Bus Transceiver idt74FCT621TS0 is a commercial part that was up-screened by IDT to meet the industrial temperature range (-40 to +85°C). The part was marked by the addition of the -5100 that refers to an IDT internal process flow that specified the up-screening. These up-screened parts were used for PV at insignificant cost penalty.

Motorola (MCM6246-20), 4 megabyte SRAM has an active power of 200 ma and a standby power of 15ma and produces 363mW with a 33% duty cycle. The FEC/PNP design has clocking that would allow a 25-nsec part to be used. IBP-MPCL derated this, and chose a 20-nsec part.

The Motorola SRAM has slower timing in a few instances (output hold, write disable) than the military part. This is not a problem in the application. For back-to-back write-reads, with zero wait states, these 2 times would not be an issue because there is a complete 50-nsec cycle between states. An external test house (Space Electronics) performed A.C. characteristic and functional testing on PV SRAMs over -40 to +85C. For the 516 parts tested there were 0 failures and all operated within the 20-nsec access time, even at cold.

4.3.2 Electrical

4.3.2.1 Power Consumption

Power consumption analysis was performed for parts that were changed from the military design. Parts that were substituted with electrical equivalents in industrial packaging were not analyzed, and the baseline numbers were used. The power consumption analysis was used as an input to the thermal analysis. Table 4.3.2.1-1 is a summary of the power consumption analysis for the parts that were changed.

Table 4.3.2.1-1 Power Consumption Analysis Summary

Part	Characteristics	Notes
AD811AR-16 Op-Amp	100 ma max per output x 4V = 400mW if terminating in 50 ohm, then 320mW or 16 ma into 75 ohm could be used. Only one output transistor on at a time. Max Junction temperature = θJA = 85°C/W Operating Temp -40 to +85C Storage Temp -65 to 125C	**Only one amp per package is being used to reduce heat**
CLC412 Op-Amp	50mW per amplifier typical x2 = 100mW 12.8ma max per amplifier x 5v x 2 amplifier per pkg = 128mW Max Junction Temperature = 175C Operating Temp -40 to +85C Storage Temp -65 to 150C	
LT1127 Op-Amp	2.7 ma per output x 12V = 129.6 mW Only one output transistor on at a time. Max Junction temperature = not given Operating Temp -40 to +85C Storage Temp -65 to 150C	
LT1362 Op-Amp	5ma max per amplifier x 12v x 2 amplifier per pkg = 120mW Max Junction Temperature = 150C Operating Temp -40 to +85C, Storage Temp -65 to 150C	**Both in the package are being used.**
Additional Resistors for pull-downs	For buffers, idt FCT input stage = - 15ua for logic low 2000 ohm @ 15 ua = .03V >> acceptable .5v Power = .45mW << 1/10 W rating	
Motorola MCM6246-20	Active = 200 ma max Standby = 15 ma Using 80% active Power = .8(.2 x 5.0) + .2(.015 x 5.0) = 815mW IDT7164S15TI 8kx8; 15nsec part Standby = 20 ma max; 100mW Active = 180 ma max; 900mW scaled message traffic = 100 nsec reads, 100nsec writes yields effective 50nsec operation Ptyp (using 1/3 active) Ptyp = .33(.9) + .66(.1) = 363mW Operating Temp 0 to 70C, Storage Temp -55 to 150C	
Atmel AT28C010 128kx8	Active = 80ma Standby = 300 uA Power = use standby numbers (downloaded to SRAMs) P = 300E-6 x 5.0 = 1.5 mW Active power = 80ma x 5.0 = 400mW, 5 wait states = 80 mW Operating Temp -40 to +85C, Storage Temp -65 to 150C	
Atmel AT29C010 128kx8	Active = 50ma Standby = 300 uA Power = use standby numbers (downloaded to SRAMs) P = 300E-6 x 5.0 = 1.50 mW Active power = 50ma x 5.0 = 250mW, but used at 5 wait states; 50mW each Operating Temp -40 to +85C, Storage Temp -65 to 150C	
Buffer IDT74FCT244ATU	Current = 1.5ma Power = 7.5 mW Operating Temp -40 to +85C, Storage Temp -55 to 125C	

4.3.2.2 Circuit Tolerance Analysis

The military designs had a memory requirement of 256kx40. The military program satisfied this requirement using ten 128kx8 Paradigm SRAMs that were packaged inside the DSP multi-chip module. In the redesign effort, the MCM was broken out into discrete components. The IBP-MPCL solution reconfigured the memory to use five 512kx8 SRAMs. This saved board area, reduced the amount of board routing, and increased available memory by 50%. Table 4.3.2.2-1 is a comparison of the electrical specifications of various parts evaluated in this trade study. The Motorola (MCM6246-20) SRAM was used for PV.

Table 4.3.2.2-1 SRAM Specification Comparison

Characterisitc	Paradigm	Paradigm	White	White	NEC	Motorola	units
Size	128KX8	128KX8	512KX8	512KX8	512KX8	512KX8	
P/N	PDM41024-20	PDM41024-25	WMS512K8-20	WMS512K8-25	uPD434008-20	MCM6246-20	
TEMP	INDUS	INDUS	INDUS	INDUS	Indus	Commercial	
ACTIVE PWR	175	175	130 @ 5MHz	130 @ 5MHz	190 max	200max	mA
STBY PWR	10	10	15@5MHz	15@5MHz	10	15	mA
Capac in	8	8	20	20	6	6 data, 8 for en	pf @25C, 1MHz
Capac out	8	8	20	20	10	8	pf @25C, 1MHz
Read cycle time tRC	20min	25min	20 min	25 min	20min	20min	ns
Address access time tAA	20max	25max	20 max	25 max	20max	20max	ns
Chip Enable Access time tACE	20max	25max	20max	25 min		20max	ns
Output hold from address change tOH	3min	3min	0min	0min	3min	**5min**	ns
Chip Enable to output in low Z tLZCE	5min	5min	2min	2min	3min	5min	ns
Chip disable to output in highZ tHZCE	10max	10max	10max	12max	8max	9max	ns
Chip enable to pwr up time tPU	0min	0min	not spec'd	not spec'd	not spec'd	0min	ns
Chip disable to pwr down tPD	20max	25max	not spec'd	not spec'd	not spec'd	20max	ns
Output enable access time tAOE	8max	8max	10 max	**12 max**	8max	6max	ns
Output enable to output in low Z tLZOE	0min	0min	0min	0min	0max	0min	ns
Output disable to output in high Z tHZOE	8max	10max	10max	**12 max**		0min/9max	ns
Write cycle tWC	20min	25min	20 min	25 min	20min	20min	ns
Chip enable to end of write tCW	15min	15min	14min	15min	14min	15min	ns
Address valid to end of write tAW	15min	15min	14min	15min	14min	15min	ns
Address set up time tAS	0min	0min	0min	0min	0min	0min	ns
Address hold from end of write tAH	0min	0min	0min	0min	**3min**	0min	ns
Write pulse width tWP	15min	15min	14min	15min	12min	15min	ns
Data setup time tDS	10min	10min	10min	10min	10min	10min	ns
Data hold time tDH	0min	0min	0min	0min	0min	0min	ns
Write disable to output in low Z tLZWE	0min	0min	3min	**4min**	0min	**5min**	ns
Write enable to output in high Z tHZWE	8max	10max	9 min	10min	0min,8max	0min,9max	ns
PRICE $$	$114	$114	$247	$247	$94	$46	

A trade study was also performed for the Atmel EEPROM devices. Table 4.3.2.2-2 shows a comparison of the electrical characteristics. Switching from the military EEPROM to an industrial FLASH type memory would reduce the cost from $165 to $38 for each part. This savings is magnified by the fact that each module has a minimum of 5 FLASH devices. The difference in the two memory types is that the FLASH does not have the ability to accept individual byte writes. The FLASH memories must have a page written at a time, or the

rest of the page will be overwritten with "FF". The software team determined that byte writes are not required, and that a move to FLASH memories was feasible.

Table 4.3.2.2-2 FLASH Specification Comparison

Parameter	Type of ATMEL Prom					Notes
	AT28C256	AT28C010	AT29C256	AT29C257	AT29C010	
Type	EEPROM	EEPROM	FLASH	FLASH	FLASH	
size	32kx8	128kx8	32kx8	32kx8	128kx8	
features				same pinout as 128kx8		
program page	1 thru 64	1 thru128	64 only	64 only	128 only	
access time	150 ns	120/150	120/150	120/150	120/150	
active Ic	3ma	80ma	80ma	50ma	50ma	
stdby Ic	200ua	300ua	300ua	300ua	300ua	
Cin (max)	6pf	10pf	6pf	6pf	6pf	
Cout (max)	12pf	12pf	12pf	12pf	12pf	
tWP (write PW)	100 ns	100 ns	120ns min	120nsec	90ns min	
tDH (data hold time for polling	0 ns	10ns min	0 ns	0 ns	10ns min	all 10 ns for toggle bit
tOEh output enable hold time-polling	0 ns	10ns min	10ns min	10ns min	10ns min	all 10 ns for toggle bit
byte cycle width high -for prog	150 us max	150 us max	150 us max	150 us max	150 us max	

4.3.2.3 Signal Integrity Analysis

Quad Analysis was not performed on the modules due to schedule incompatibilities of the ASIC pin-outs and hardware builds. Spreadsheet analyses were performed to determine setup and hold timing margins. Wherever the margins were less than 2 nsec, faster components were used. A minimum of 10 % timing derating was maintained on the clock signals. The complete DSP to SRAM interface was re-analyzed because of tight margins. Positive timing margins were maintained throughout the design.

4.3.2.4 Decoupling Analysis

Decoupling capacitors act as reservoirs that provide switching power to the digital outputs. The number of decoupling capacitors used on the baseline provide a maximum power supply deviation of 50 mV. Approximately the same number of decoupling capacitors were used for the IBP-MPCL boards. The placement varied due to new board layouts and the breakup of the DSP MCM (which contained 24 decoupling capacitors). Capacitors were chosen that were TRW AEN standard parts.

4.3.2.5 ASIC PIN Assignments

Two processes were used for the conversion of the military quad flat pack parts into plastic ball grid array (PBGA) packages. For the LSI parts, the LSI tool CDME was used. IBM was chosen to repackage the Motorola ASICs. IBM created new PBGA layouts and pin assignments according to layout guidelines provided by TRW-ASD.

The LSI die developed for the military program were used along with the CDME tool in order to create a die pad to bond finger mapping. The tool is designed so that as the signals are laid out, the power and grounds are placed to balance the power and ground ring. Layout limitations prevent the engineer from placing too many adjacent signals without power/ground breaks. The MAME ASIC had special power and ground cuts that allowed one portion of the design to be powered separately. This feature had to be added at a later stage of the layout process because the CDME process could not account for it. The LSI Package Selector Guide Catalog was used to choose an available standard PBGA package that corresponds with the die size and pin-out requirements. The catalog was used to assign BGA pin-outs to each signal after bond finger mapping.

For the ASICs packaged by IBM, a different approach was used. IBM created the package layout using the Motorola die maps, package preferences, critical routing signals (for within the BGA substrate), and a list of signals requiring adjacent power or grounds. The output of this process was a signal name to BGA pin map drawing. IBM used off the shelf Open-Tool Packages to create the custom package layout. These placements were checked for signal omissions, naming, routability and breakout.

Both the LSI and IBM processes were performed iteratively, and many checks of the pin maps were made. Upon completion of the ASIC pin assignments, the data was added to each of the ASIC's SCD drawings. The pin mapping file for the symbol on the schematic was generated by the component librarian using this pin assignment data.

4.3.2.6 DFMEA (Design Failure Mode & Effects Analysis)

A DFMEA was performed on a sample circuit of the IBP PNP module. The intent was to compare the methodology of the automotive / commercial DFMEA with military DFMEA methodology which is based on MIL-STD-217 (Reliability Prediction of Electronics Equipment). Originally, the plan was to develop DFMEA analyses on all the circuits of both PNP and RF/FEC modules.

Due to resource limitations, it was decided to perform a "proof of concept" analysis on one circuit and develop recommendations based on that analysis.

The avionics methodology provides a top down analysis that starts at the system level and moves to the module level. For the system, a 100% screened and functional module (LRM - line replaceable module, or LRU - line replaceable unit) is assumed. A system failure level is set which is based on the combination of the module's component reliability data. The component reliability data established a mean time between failure (MTBF) for each of the components. The data is collected and a DFMEA is created once for the entire program. It is typically performed during the design phase of the program. MIL-STD-217 is contractually required for most military programs.

The automotive methodology provides a "bottoms-up" analysis from the component level. It addresses both board level design and manufacturing processes. The idea is to design out board functional weaknesses that cause producibility and in-service problems. The board is not considered to be 100% functional, but it is shown to be as error-free as possible through design evaluation, in-circuit testing, module level testing, design verification testing, and production validation testing. The result of this produces the highest quality / lowest production cost to customer. The document is a living document containing action plan and results. This reduces failure rates through actively working issues and making changes to design, manufacturing, and test processes based on results. The failures and effects categories are similar to the military in format. The DFMEA is a requirement for all automotive customers.

Both the avionics and automotive methodologies address function, potential failure modes, failure detection methods and design controls. The automotive DFMEA discusses recommended actions, whereas the avionics contains compensating provisions. The automotive DFMEA uses RPN (Risk Priority Number) which is calculated from by multiplying the severity of a failure times its occurrence times its ability to be detected. The lower the RPN number the better. High RPN numbers should be addressed by the designers.

The automotive DFMEA lacks local effects of the failure, failure mode indicator, and output identification name (signal name or grouping identifier). The system level DFMEA for the automobile is required for the end effect of the function.

The avionics DFMEA lacks severity and classification columns. All portions of the module or board that is being tested are determined to be at the same severity level. Also, the occurrence of the failure is lacking. It does not break

out whether the failure is found during fabrication, test or in field. Since the avionics plan is a one time plan, and not a living document, it lacks action plans, actions taken and completion dates, as well as follow-up results.

The automotive DFMEA appears to be the more effective of the two approaches. It requires action plans, responsibilities, and results for areas of high risk, failure, or return. It is a living document that requires updates as the processes and products change and mature. It develops a history on the product, as reliability data becomes available from either testing or from the field. With the avionics low volume and high mix production, component failure feedback is not readily available. Predictions have to be made from test data. Accelerated tests, built in test, and high level functional test is required for feedback of data. The DFMEA must be developed by the design team at the time of design. The developers must understand the design, functionality and use of the product. The analysis must be divided into areas of expertise. Sections will be done from the electrical, mechanical, software, and process engineers. This is a tool to improve the product and not just a program status report. The automotive DFMEA is time consuming to prepare, approximately one hour of analysis per line item. On the IBP-MPCL program, since the ASIC design was already completed, it was not feasible to create a complete DFMEA. Where the RPN numbers were high, the design already had a good detection mechanism, thus no corrective actions were taken. A sample was created and is shown below using the PNP bus signals.

Table 4.3.2.6-1 Sample DFMEA

Subsystem: PNP					Design Responsibility: Jim Wilk					Design FEMEA Number: TBD						
Model Years: All					Key Date: 8/1/96					Page 1of TBD						
										Prepared by: J J Wilk						
										FMEA Date: 2/12/96 Rev O.D.						
Core Team: J Wilk-Elec, F Bartlett-Parts, B. Lage-Mech, L Jindra-Mfgrr, R Hill-Ops																
												Action Results				
Item Function	**Potential Failure Mode**	**Potential Effect(s) of failure**	**SEV**	**CLASS**	**Potential Cause(s) Mechanism of Failure**	**Occur**	**Current Design Controls**	**DETEC**	**RPN**	**Recommended Action(s)**	**Responsibility & Target Completion Date**	**Actions Taken**	**SEV**	**OCC**	**DET**	**RPN**
CNI Bus Data Lines	Stuck High/ CBIU	CBIU QUEUE Output buffer failure - causes bus data bit to be stuck HIGH when PNP is Granted Bus talker status	8		CBIU output drivers have stuck at High fault.	3	Module reports parity failure during UHF/VHF Loopback (PBIT), SBIT, IBIT, BIST - detect CBIU failure	1	24	NONE	N.A.					
					Circuit board has via short or trace short leading from 5V plane to CNI data bus lines	6	Module reports parity failure during UHF/VHF Loopback (PBIT), SBIT, IBIT, BIST - detect CBIU failure	1	48	NONE	N.A.					
CNI Bus Data Lines	Stuck Low/ CBIU	CBIU QUEUE Output buffer failure - causes bus data bit to be stuck LOW when PNP is Granted Bus talker status	8		CBIU output drivers have stuck at Low fault.	3	Module reports parity failure during UHF/VHF Loopback (PBIT), SBIT, IBIT, BIST - detect CBIU failure	1	24	NONE	N.A.					
					Circuit board has via short or trace short leading from DGND to CNI data bus lines	6	Module reports parity failure during UHF/VHF Loopback (PBIT), SBIT, IBIT, BIST - detect CBIU failure	1	48	NONE	N.A.					
					Short in J1 connector between DGND and CNI data lines	5	Module reports parity failure during UHF/VHF Loopback (PBIT), SBIT, IBIT, BIST - detect CBIU failure	1	40	NONE	N.A.					
CNI Bus Data Lines	garbled output / CBIU, NTL Refer gen, Nar Band Proc	Incorrect transfer of data between Narrow Band Processor and CNI Bus Interface Unit (CBIU)	8		CBIU or NBP ASIC at fault or bad NTL ref Generator	3	Module parity may pass (PBIT); SBIT, IBIT - BIST is req'd to determine which ASIC	2	48	NONE	N.A.					
					Short between any adjacent data lines on circuit board	7	Module reports parity failure during UHF/VHF Loopback (PBIT), SBIT, IBIT - detect CBIU failure	1	56	NONE	N.A.					
					Short between adjacent signals at connector	6	Module reports parity failure during UHF/VHF Loopback (PBIT), SBIT, IBIT - detect CBIU failure	1	48	NONE	N.A.					

4.3.2.7 EMI/EEE

A deviation analysis of the Electromagnetic Interference and Electronic and Electromagnetic Effects (EMI/EEE) due to design changes was performed. A full analysis of the EMI/EEE requirement has already been performed on the military contract. The military contract will follow this by performing full EMI/EEE testing at the IAR level. These tests will include conducted emissions, conducted susceptibility, near field emissions, magnetic susceptibility, and radiated susceptibility. The IBP-MPCL design changes affecting EMI are the switch from ceramic cavity packages on the ASICs to plastic ball grid arrays, and the change in cover material. Reviewing the military contract data analysis, a minimum of 40 db shielding was required by the covers and the packaging in order to achieve acceptable EMI limits. Testing was performed on the IBP-MPCL and military style covers in order to validate the IBP-MPCL cover design and to determine shielding effectiveness.

4.3.3 Mechanical

4.3.3.1 Weight

The repackaging of the military version of these modules provided an opportunity for weight savings. The primary areas where weight savings were attained are in the thermal plane, module covers and the circuit components. A comparison of the weights between the military and IBP-MPCL modules is shown in Table 4.3.3.1-1 and is repeated graphically in Figure 4.3.3.1-1.

Table 4.3.3.1-1 Weight Comparison from Baseline to IBP-MPCL

	F-22 Baseline	IBP
Thermal Plate	0.211	0.158
PWBs	0.275	0.266
Covers	0.186	0.148
Circuit Components	0.357	0.205
F22 Common Hdwre	0.190	0.190
Misc. Other	0.161	0.045
Total Weight	1.38	1.01

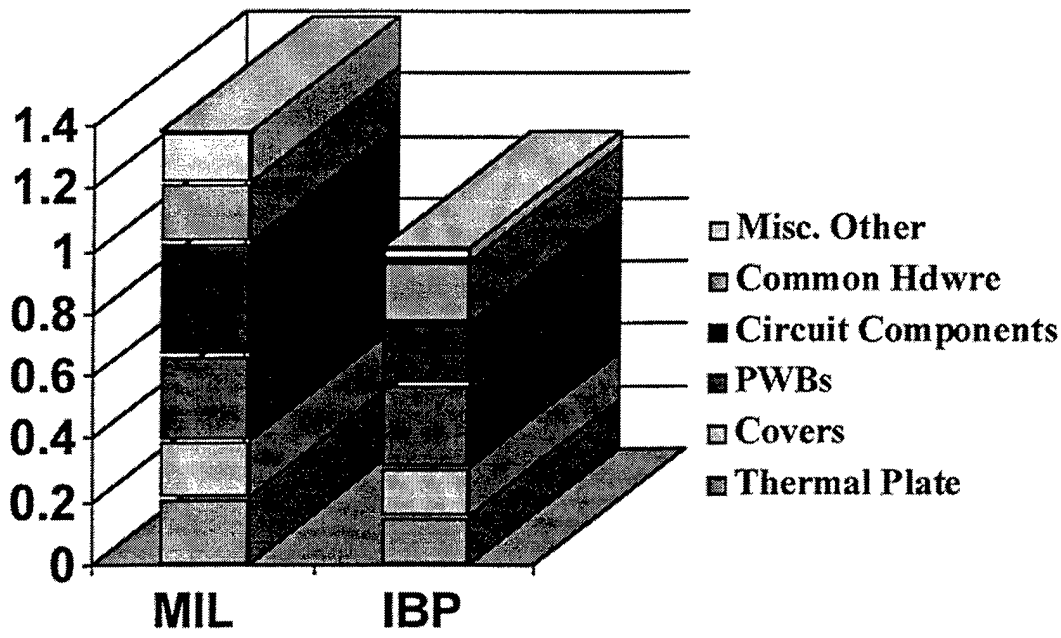


Figure 4.3.3.1-1 Weight Comparison from Baseline to IBP-MPCL

4.3.3.2 Durability Analysis

Durability analysis is a physics of failure approach to time dependent failure modes. The areas of primary concern for long term durability of this design were low cycle fatigue of plated through holes, which can cause cracking in the copper barrel due to cyclic loading, and high and low cycle fatigue of BGA solder joints, which can result in solder joint failure from vibration and thermal cycling loads, respectively. These analyses are compared to empirical results and the analyses updated accordingly.

Durability fatigue analysis is based on a damage index analysis. In this analysis, the number of cycles for a cyclic induced stress, strain or displacement that an environment induces is divided by the cycles required to fail the part at that same stress, strain or displacement level. This value is referred as the damage index. The sum of the damage indices for each environment is the cumulative damage index (CDI). CDI includes all environments that induce fatigue and is the sum of the thermal damage index (TDI) and the vibration damage index (VDI). A CDI of 1.0 implies an expected failure. The goal of the program is to demonstrate an analytical CDI of 0.5 and empirically show a CDI of 1.0, where the cycles to fail the part are set equal to one lifetime.

4.3.3.2.1 Plated Through Holes

Durability analysis for the plated through holes is developed from Lambert's method. Lambert has shown that the mean fatigue life expressed as a number of cycles N to failure is estimated according to:

$0.6598E_t'N^{-0.6} + 0.0015N^{-0.12} - K\Delta\varepsilon = 0$, Where

$E_t' = 0.53127t^{1.661276}$

t = the thickness, in mils, of the plated through hole barrel

K = strain concentration factor

Lambert's method is based on the classic Coffin-Manson strain-life relation:

$\frac{\Delta\varepsilon}{2} = \frac{\sigma_f'}{E}(2N_f)^b + \varepsilon_f'(2N_f)^c$, Where

$\Delta\varepsilon$ = amplitude of total applied strain range

σ_f' = fatigue strength coefficient

b = fatigue strength exponent

ε_f' = fatigue ductility coefficient

c = fatigue ductility constant

E = modulus of elasticity

N_f = number of cycles to failure.

Using the above equations, K (strain concentration factor) is "tuned" to correlate the failure predictions with empirical data gathered from previous testing. With this model, the actual expected environments are inputs and predictions of the fatigue capability of the plated through holes to different service environments were performed. Figure 4.3.3.2.1-1 shows the results of the fatigue analysis as a function of plating thickness. In order to achieve a DI of 0.5, 1.6 mils of copper plating is required. Because of the sensitivity of the damage index to the plating thickness, 2.0 mils was selected as the requirement to insure meeting the requirement.

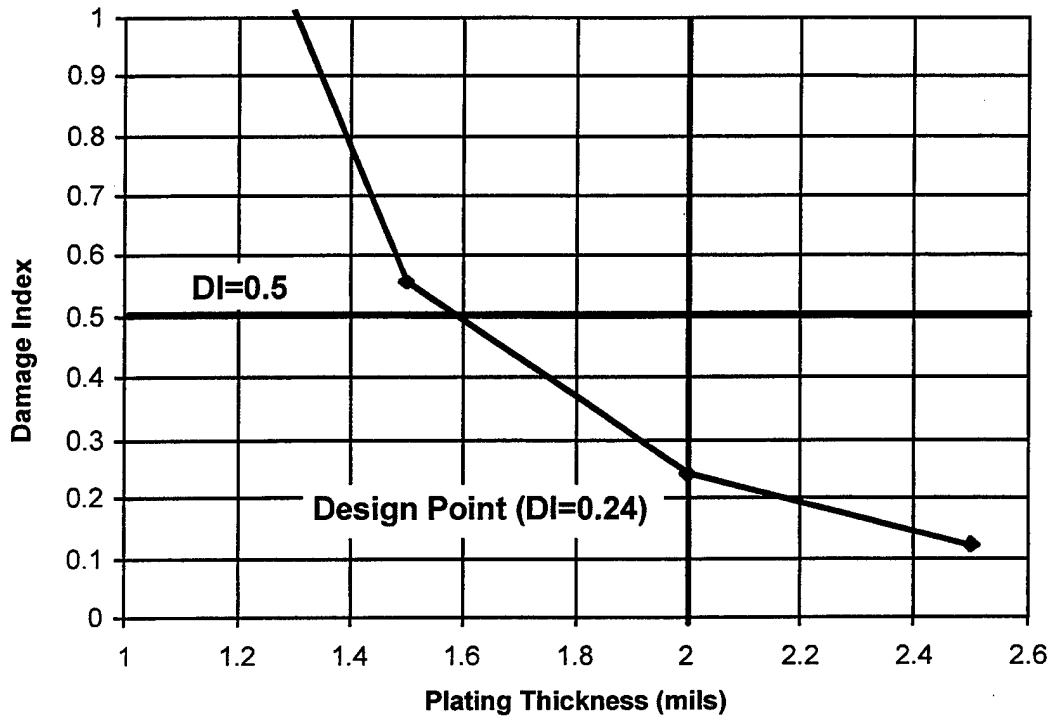


Figure 4.3.3.2.1-1 Plated thru Hole Durability vs. Plating Thickness

4.3.3.2.2 BGAs High Cycle Fatigue

High cycle fatigue durability analysis for the BGA solder joints is developed from Steinberg's method. Steinberg has shown that the fatigue life of the solder joint for a leadless component expressed as a number of cycles N to failure is estimated according to:

$$N_f = N_z * \left(\frac{Z_{20e6}}{Z_{act}}\right)^b \text{, Where}$$

N_f = Cycles to failure at calculated deflection

N_z = Cycles to failure at Z (20e6)

Z_{act} = Calculated deflection

Z_{20e6} = Allowable deflection for 20e6 cycles to failure

b = material fatigue constant.

Steinberg developed the relationship for the allowable deflection at 20e6 cycles to failure as:

$$Z_{20e6} = \frac{0.00022 * B}{C * h * r * \sqrt{L}}$$, Where

B = Length of PWB parallel to component length (in)
L = Length of component edge (in)
C = Component type factor (2.25 for LCC, 1.0 for leaded)
r = Position factor (1.0 for PWB center)
h = PWB thickness (in)

The key to "tuning" this analysis is using the correct component factor. For BGAs, the component type factor was unknown. Initial testing results indicated that a VDI less than 0.2 would be realized. Due to the robustness of the design in regards to vibration, not enough failure data was accumulated to accurately determine the correct component factor.

4.3.3.2.3 BGAs Low Cycle Fatigue

Low cycle fatigue durability analysis for the BGA solder joints is developed from Englemaier's method. Englemaier has shown that the mean fatigue life of the solder joint for a leadless component expressed as a number of cycles N to failure is estimated according to:

$$N_f = \frac{1}{2}\left(\frac{F}{2\varepsilon_f'}\frac{L_D \Delta\alpha \Delta T_e}{h}\right)^{\frac{1}{c}}$$, Where

$$c = -0.442 - 6x10^{-4}\,\overline{T}_{sj} + 1.74x10^{-2}\ln\left(1 + \frac{360}{t_D}\right)$$, And

c = fatigue ductility exponent
F = Empirical factor
h = solder joint height
$2L_D$ = max distance between component solder joints
$\overline{T}_{sj}$ = mean cyclic solder joint temperature
t_D = half cycle dwell time in minutes
$\Delta\alpha$ = component to substrate CTE mismatch
ΔT_e = equivalent cyclic temperature swing
ε_f' = fatigue ductility coefficient

Using the above equations, F (Empirical factor) has been "tuned" to correlate the failure predictions with empirical data gathered from previous testing on LCCs. This gives some preliminary analysis capabilities for BGAs, assuming similar empirical factors. The results of DOE #1 and DOE #2 corrected the

assumed emperical factor for PBGAs. With this model, the actual expected environments are used as inputs and predictions of the fatigue capability of the BGA solder joints to different service environments were performed. Table 4.3.3.2.3-1 shows the results of the fatigue analysis for the various BGAs used on these modules for the environments, the materials of the IBP-MPCL design and empirical factors "tuned" to a 50% failure rate of DOE #1 hardware. This empirical factor is still assumed to be conservative in that DOE #1 had many noise factors that would cause early failures that will be designed out based on the results of DOE #1.

Table 4.3.3.2.3-1 Fatigue Analysis Results with F Tuned to DOE #1 Data

	CTE Sub	CTE Comp	DimX	DimY	T C	T B	SJ ht	Emp	TDI
DMAD	17	18.5	0.708	0.708	72.6	69.8	0.016	1.74	**0.77**
C31	17	18.5	0.708	0.708	73.3	71.9	0.016	1.74	**0.57**
MTC	17	15	0.826	0.826	61.6	60.7	0.023	1.71	**0.17**
NBP	17	18.5	0.950	0.950	64.8	63.4	0.023	1.71	**0.37**
MAME	17	15	1.200	1.200	56.2	54.4	0.023	1.69	**0.23**
CBIU	17	15	1.200	1.200	66.4	64.6	0.023	1.69	**0.36**
RTP	17	18.5	1.250	1.250	67.5	65.8	0.023	1.69	**0.79**
DSP	17	18.5	1.250	1.250	66.7	65.0	0.023	1.69	**0.77**

4.3.3.3 Thermal Analysis

Thermal analysis was performed on each of the modules to determine the junction temperatures of the microcircuits. The primary steps in the analysis are as follows:

1) Determine thermal plate temperature as a function of component location. This is done using finite differences (could also use finite elements). Inputs to this analysis are the effective thermal conductivity of the board/adhesive/core combination, module boundary conditions at the rails and the component power levels at different nodes or elements of the model.

2) Determine junction temperature of active components. This is done using a resistive flow spreadsheet model. Thermal plane temperatures are known from step 1 and die powers are also known. Each material in the path between the die junction and case and between the case and thermal plate is assigned a thermal resistance based on material thermal conductivity and element

geometry. From this model, resistance between the junction and case (Rjc) and resistance between the case and thermal plane (Rctp) are calculated. These are combined to calculate total resistance and junction temperature.

Table 4.3.3.3-1 through 4.3.3.3-4 show the summary results of this thermal analysis.

The incorporation of PEMs in the design requires improved thermal conductivity in the core. This is primarily due to the higher thermal resistance between the junction and case (Rjc) for PEMs versus ceramic military parts. For PEMs that run hot, including thermal adhesive under the parts can reduce junction temperatures. This will typically reduce the thermal resistance between the part case and the thermal plane (Rc-tp) by a factor of two.

Ball grid array packages can have a relatively low Rjc (typically, 2-4 °C/watt) due to the excellent thermal coupling provided by the solder balls and vias directly under the die. If a peripheral ball type part is used and there are no thermal vias and balls placed under the die, the Rjc can easily be as high as 25 to 30°C/watt.

Table 4.3.3.3-1 Thermal Analysis Results Summary for PNP Board A

THERMAL ANALYSIS/DESIGN DATA REPORT
IBP PROCESSOR, COMMUNICATION - NAVIGATION DATA (PNP) MODULE
CD-2287/ASQ-220

TRW

Board A, Nom. Power = 10.33 Watts

						Power Dissipation		Thermal Resis		Predicted Temperatures. for F-22 Environment							
	Ref			Package		MCM / Subtotal	Die	R j/c	R c/tp case/core	T PAO/max Norm. Ops	T max Rack Rail	T max LRM Rib	T t/plate	T case	T j Norm. Ops	T j Ground Ops	T case Max. Allow
em #	Des	Description	Part Number	Style	Die Size	(W)	(W)	°C/W)	(°C/W)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)
1		MCM Breakout				4.320											
	U5	DSP ASIC	54H4509	BGA 352		-	0.809	3.12	3.05	35.0	41.2	49.1	65.1	67.6	70.1	90.1	105.0
	U13	C31 Signal Processor	54H4513	BGA 169		-	1.688	3.41	3.79	35.0	41.2	49.1	65.7	72.1	77.9	97.9	105.0
	U2	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	41.2	49.1	65.9	68.5	73.5	93.5	105.0
	U3	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	41.2	49.1	66.3	69.0	73.9	93.9	105.0
	U8	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	41.2	49.1	66.8	69.5	74.4	94.4	105.0
	U12	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	41.2	49.1	67.2	69.9	74.8	94.8	105.0
	U14	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	41.2	49.1	67.3	69.9	74.9	94.9	105.0
	U17	Octal Buffer	IDT4FCT255ATSO-5100	SOIC 20		-	0.008	6.35	31.76	35.0	41.2	49.1	67.3	67.6	67.6	87.6	105.0
2	U1	128 x 8 Flash	AT29C010A-12JI	PLCC 32	.232 x .358	0.250	0.050	8.86	12.57	35.0	41.2	49.1	65.7	66.3	66.8	86.8	105.0
	U6	128 x 8 Flash	AT29C010A-12JI	PLCC 32	.232 x .358		0.050	8.86	12.57	35.0	41.2	49.1	66.1	66.7	67.1	87.1	105.0
	U7	128 x 8 Flash	AT29C010A-12JI	PLCC 32	.232 x .358		0.050	8.86	12.57	35.0	41.2	49.1	66.4	67.0	67.5	87.5	105.0
	U11	128 x 8 Flash	AT29C010A-12JI	PLCC 32	.232 x .358		0.050	8.86	12.57	35.0	41.2	49.1	66.8	67.4	67.9	87.9	105.0
	U16	128 x 8 Flash	AT29C010A-12JI	PLCC 32	.232 x .358		0.050	8.86	12.57	35.0	41.2	49.1	67.1	67.7	68.1	88.1	105.0
3	U4	Narrowband Proc. (NBP) ASIC	C884803-1	BGA 256		1.250	1.250	3.00	3.48	35.0	41.2	49.1	63.3	67.6	71.4	91.4	105.0
4	U18	Tranceiver (Scan Line Driver)	SCAN18541TSSC	SSOP 56	.161x.147	0.100	0.050	14.15	7.68	35.0	41.2	49.1	63.3	63.6	64.3	84.3	105.0
	U19	Tranceiver (Scan Line Driver)	SCAN18541TSSC	SSOP 56	.161x.147		0.050	14.15	7.68	35.0	41.2	49.1	65.8	66.1	66.9	86.9	105.0
5	U9	12 Bit D/A Converter	DAC813AU	SOIC 28	.140 x .185	1.320	0.440	27.80	14.66	35.0	41.2	49.1	65.6	72.0	84.2	104.2	105.0
	U10		DAC813AU				0.440	27.80	14.66	35.0	41.2	49.1	60.8	67.2	79.4	99.4	105.0
	U15		DAC813AU				0.440	27.80	14.66	35.0	41.2	49.1	63.4	69.8	82.1	102.1	105.0
6	U20	CNI Bus Interface Unit (CBIU) ASIC	C884805-1	BGA-313	.591 x .591	1.600	1.600	2.51	3.05	35.0	41.2	49.1	65.0	69.9	73.9	93.9	105.0
7	U22	Maint. & Test Contoller (MTC) ASIC	C884806-1	BGA-225	.512 x .512	0.800	0.800	2.73	3.72	35.0	41.2	49.1	65.2	68.2	70.4	90.4	105.0
	U23	128 x 8 EEProm	AT28C010(E)-12JI	PLCC 32	.232 x .358	0.200	0.080	8.86	12.57	35.0	41.2	49.1	67.0	68.0	68.8	88.8	105.0
8	U21	16 Bit Buffer/Driver	SN74ABT16244ADL	SSOP 48	.057 x .137	0.115	0.115	26.39	9.00	35.0	41.2	49.1	67.0	68.0	71.1	91.1	105.0
9	U24	Octal Register (Transceiver)	SN74ABT8646DW	SOP 28	.139 x .167	0.115	0.115	23.02	14.24	35.0	41.2	49.1	65.6	67.2	69.9	89.9	105.0
10	AR1	Quad Operational Amplfier	LT1127CS	SOL 16	.106 x .163	0.258	0.129	23.09	12.87	35.0	41.2	49.1	60.5	62.1	65.1	85.1	105.0
	AR2		LT1127CS				0.129	23.09	12.87	35.0	41.2	49.1	62.8	64.5	67.5	87.5	105.0
			Board A Total Power			10.33											

XXXX Hottest Component

Table 4.3.3.3-2 Thermal Analysis Results Summary for PNP Board B

THERMAL ANALYSIS/DESIGN DATA REPORT
IBP PROCESSOR, COMMUNICATION - NAVIGATION DATA (PNP) MODULE
CD-2287/ASQ-220

TRW

Board B, Nom. Pow 24.62 Watts

						Power Dissip		Thermal Resis		Predicted Temperatures. for F-22 Environment							
	Ref			Package		MCM / Subtotal	Die	R j/c	R c/TC	PAO/m	T max	T max	t/plat	T case	T j	T j	T case
										Norm. Op	Rack Rai	RM Rib			Norm. Op	round O	Max. Allow
tem	De	Description	Part Number	Style	Die Size	(W)	(W)	°C/W	(°C/W)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)
1	U1	Receive/Xmit Proc (RTP)	C884801-1	BGA 352	589 x .58	6.000	3.000	3.12	3.05	35.0	41.2	49.1	65.6	74.7	84.1	104.1	105.0
	U2						3.000	3.12	3.05	35.0	41.2	49.1	65.2	74.4	83.7	103.7	
2	U4	SRAM, 8K x 8	IDT7164S15YI	SOJ 28	139 x .17	1.360	0.340	13.53	7.40	35.0	41.2	49.1	63.4	65.9	70.5	90.5	105.0
	U5						0.340	13.53	7.40	35.0	41.2	49.1	65.4	67.9	72.5	92.5	
	U9						0.340	13.53	7.40	35.0	41.2	49.1	65.7	68.2	72.8	92.8	
	U10						0.340	13.53	7.40	35.0	41.2	49.1	63.8	66.3	70.9	90.9	
3	U3	PROM, 32K x 8	CY7C277-40JC	PLCC 32	.197 x.197	2.080	0.520	10.87	15.53	35.0	41.2	49.1	66.8	74.9	80.6	100.6	105.0
	U6						0.520	10.87	15.53	35.0	41.2	49.1	66.6	74.7	80.3	100.3	
	U7						0.520	10.87	15.53	35.0	41.2	49.1	67.2	75.3	81.0	101.0	
	U8						0.520	10.87	15.53	35.0	41.2	49.1	66.5	74.5	80.2	100.2	
4	U14	Quad Diff. Line Driver	DS26C31TM	SOP 16L	.064x.074	0.120	0.060	6.35	20.88	35.0	41.2	49.1	60.4	61.7	62.1	82.1	105.0
	U18						0.060	6.35	20.88	35.0	41.2	49.1	60.3	61.6	61.9	81.9	
5	U11	Wide Band A/D Conv. (DN	C884804-1	BGA 169	368 x .36	14.580	2.430	3.41	3.79	35.0	41.2	49.1	64.9	74.1	82.4	102.4	105.0
	U12						2.430	3.41	3.79	35.0	41.2	49.1	68.2	77.4	85.7	105.7	
	U13						2.430	3.41	3.79	35.0	41.2	49.1	67.1	76.3	84.5	104.5	
	U15						2.430	3.41	3.79	35.0	41.2	49.1	65.3	74.5	82.8	102.8	
	U16						2.430	3.41	3.79	35.0	41.2	49.1	67.0	76.2	84.5	104.5	
	U17						2.430	3.41	3.79	35.0	41.2	49.1	63.9	73.1	81.4	101.4	
6	AR1	Quad Operatioinal Amplifi	LT1127CS	SOL 16	106 x .16	0.470	0.094	7.33	20.07	35.0	41.2	49.1	60.5	62.4	63.0	83.0	105.0
	AR2						0.094	7.33	20.07	35.0	41.2	49.1	63.3	65.1	65.8	85.8	
	AR3						0.094	7.33	20.07	35.0	41.2	49.1	60.5	62.3	63.0	83.0	
	AR4						0.094	7.33	20.07	35.0	41.2	49.1	63.3	65.1	65.8	85.8	
	AR5						0.094	7.33	20.07	35.0	41.2	49.1	66.6	68.5	69.2	89.2	
	CR1									35.0	41.2	49.1				20.0	
	CR2	Voltage Reference	LM285AM	SOP 8	040 x .04	0.005	0.005	79.40	54.11	35.0	41.2	49.1	67.0	67.3	67.7	87.7	105.0
			Board B Total Power			24.615											

73846

XXX.XXst Component

Table 4.3.3.3-3 Thermal Analysis Results Summary for FEC Board A

THERMAL ANALYSIS/DESIGN DATA REPORT
IBP CONTROL, INTERFACE (RF_FEC) MODULE
CD-109/ASQ-220

TRW

Board A, Nom. Pow 9.26 Watts

							Power Dissip		Thermal Resis		Predicted Temperatures. for F-22 Environment							
	Ref				Package		MCM / Subtotal	Die	R j/c	R c/tp case/cor	PAO/ma orm. Op	T max Rack Rai	T max LRM Rib	t/plate	T case	T j Norm. Op	T j ound Op	T case Max. Allow
tem #	Des	Qty	Description	Part Number	Style	Die Size	(W)	(W)	°C/W	(°C/W)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)	(°C)
1	U3		Synch FIFO	IDT72241L35J	PLCC 32	Assumed	1.400	0.700	15.14	12.57	35.0	38.4	42.9	50.4	59.2	69.8	89.8	105.0
	U7		Synch FIFO	IDT72241L35J	PLCC 32			0.700	15.14	12.57	35.0	38.4	42.9	50.7	59.5	70.1	90.1	105.0
2			MCM Breakout				4.320											
	U4	1	DSP ASIC	54H4509	BGA 352		-	0.809	3.12	3.05	35.0	38.4	42.9	52.1	54.5	57.0	77.0	105.0
	U12	1	C31 Signal Processor	54H4513	BGA 169		-	1.688	3.41	3.79	35.0	38.4	42.9	52.5	58.9	64.7	84.7	105.0
	U2	1	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	38.4	42.9	52.9	55.6	60.5	80.5	105.0
	U6	1	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	38.4	42.9	53.2	55.9	60.8	80.8	105.0
	U8	1	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	38.4	42.9	53.2	55.9	60.8	80.8	105.0
	U10	1	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	38.4	42.9	53.1	55.8	60.7	80.7	105.0
	U14	1	4 Meg SRAM	MCM6246WJ20	SOJ 32		-	0.363	13.53	7.40	35.0	38.4	42.9	53.2	55.9	60.8	80.8	105.0
	U18	1	Octal Buffer	IDT4FCT255ATSC	SOIC 20		-	0.008	6.35	31.76	35.0	38.4	42.9	53.4	53.6	53.7	73.7	105.0
3	U1		128 x 8 Flash	AT29C010A-12JI	PLCC 32	232 x .358	0.250	0.050	8.86	12.57	35.0	38.4	42.9	52.7	53.3	53.8	73.8	105.0
	U5		128 x 8 Flash	AT29C010A-12JI	PLCC 32	232 x .358		0.050	8.86	12.57	35.0	38.4	42.9	53.2	53.8	54.2	74.2	105.0
	U9		128 x 8 Flash	AT29C010A-12JI	PLCC 32	232 x .358		0.050	8.86	12.57	35.0	38.4	42.9	53.3	53.9	54.4	74.4	105.0
	U13		128 x 8 Flash	AT29C010A-12JI	PLCC 32	232 x .358		0.050	8.86	12.57	35.0	38.4	42.9	53.1	53.7	54.2	74.2	105.0
	U15		128 x 8 Flash	AT29C010A-12JI	PLCC 32	232 x .358		0.050	8.86	12.57	35.0	38.4	42.9	53.2	53.8	54.3	74.3	105.0
4	U21		Quad Diff Line Driver	DS96F174MW/883	FP 16	.100X.130	0.160	0.160	10.01	18.27	35.0	38.4	42.9	53.5	56.4	58.0	78.0	105.0
5	U16		Tranceiver (Scan Line Driv	SCAN18541TSSC	SSOP 56	.161x.147	0.100	0.050	14.15	7.68	35.0	38.4	42.9	50.8	51.2	51.9	71.9	105.0
	U17		Tranceiver (Scan Line Driv	SCAN18541TSSC	SSOP 56	.161x.147		0.050	14.15	7.68	35.0	38.4	42.9	52.0	52.4	53.1	73.1	105.0
6	U22		CNI Bus Interface Unit (CE	C884805-1	BGA-313	591 x .591	1.600	1.600	2.51	3.05	35.0	38.4	42.9	50.9	55.7	59.7	79.7	105.0
7	U20		Maint. & Test Contoller (MC	C884806-1	BGA-225	512 x .512	0.800	0.800	2.73	3.72	35.0	38.4	42.9	52.1	55.1	57.3	77.3	105.0
	U23		128 x 8 EEProm	AT28C010(E)-12JI	PLCC 32	232 x .358	0.200	0.200	8.86	12.57	35.0	38.4	42.9	53.4	55.9	57.7	77.7	105.0
8	U19		16 Bit Buffer/Driver	SN74ABT16244AI	SSOP 48	057 x .137	0.115	0.115	26.39	9.00	35.0	38.4	42.9	53.6	54.6	57.6	77.6	105.0
9	U24		Octal Register (Transceiver	SN74ABT8646DW	SOP 28	139 x .167	0.115	0.115	23.02	14.24	35.0	38.4	42.9	53.0	54.6	57.3	77.3	105.0
10	U11		8K x 8 NVSRAM	STK12C68S451	SOIC 28	139 x .167	0.200	0.200	23.02	14.24	35.0	38.4	42.9	51.2	54.0	58.6	78.6	105.0
				Board A Total Power			9.260											

XXX.XXst Component

Table 4.3.3.3-4 Thermal Analysis Results Summary for FEC Board B

THERMAL ANALYSIS/DESIGN DATA REPORT
IBP CONTROL, INTERFACE (RF_FEC) MODULE
CD-109/ASQ-220

TRW

Board B, Nom. Pow 8.13 Watts

Item	Ref Des	Qty	Description	Part Number	Package Style	Die Size	Power Dissip MCM / Subtotal (W)	Die (W)	Thermal Resis R j/c (°C/W)	R c/TC (°C/W)	Predicted Temperatures. for F-22 Environment PAO/ma Norm. Op (°C)	T max Rack Rai (°C)	T max LRM Rib (°C)	t/plat (°C)	T case (°C)	T j Norm. Op (°C)	T j ound Op (°C)	T case Max. Allow (°C)
1	U1		128 x 8 EEPROM	AT28C010(E)-12JI	PLCC 32	232 x .35	0.200	0.200	8.86	12.57	35.0	38.4	42.9	52.9	55.4	57.2	77.2	105.0
2	U3		MAster MEssage Intfc (M.	C884808-1	BGA 313	589 x .58	1.300	1.300	2.51	3.05	35.0	38.4	42.9	53.3	57.3	60.5	80.5	105.0
3	U2		Quad Diff Line Drvr	DS96F175MW/88	FP 16	100 x .13	0.800	0.400	10.01	18.27	35.0	38.4	42.9	53.2	60.5	64.5	84.5	105.0
	U7				FP 16	100 x .130		0.400	10.01	18.27	35.0	38.4	42.9	51.1	58.4	62.4	82.4	
4	U5		Quad Diff Line Rcvr	DS96F174MW/88	FP 16	100 x .13	0.500	0.250	10.01	18.27	35.0	38.4	42.9	53.1	57.7	60.2	80.2	105.0
	U6				FP 16	100 x .130		0.250	10.01	18.27	35.0	38.4	42.9	52.2	56.8	59.3	79.3	
5	U4		Maint. & Test Contoller (M	C884806-1	BGA-225	512 x .51	0.800	0.800	2.73	3.72	35.0	38.4	42.9	51.2	54.1	56.3	76.3	105.0
6	U9		PLL Clock Driver	IDT74FCT16827C	SSOP28	Assumed	0.090	0.090	24.70	11.54	35.0	38.4	42.9	51.0	52.0	54.2	74.2	
7	U8		Voltage Comparator	MAX913ESA	SOP 8	056 x .05	0.156	0.156	54.00	30.94	35.0	38.4	42.9	52.9	57.8	66.2	86.2	105.0
8	U10		Quad Voltage Comparator	LM139AD	SOP 14	Assumed	0.025	0.025	72.04	25.94	35.0	38.4	42.9	50.8	51.4	53.2	73.2	105.0
9	U14		Octal Bus Tranceiver	IDT74FCT621TSC	SOP 20	048 x .07	0.026	0.026	50.11	16.09	35.0	38.4	42.9	50.6	51.0	52.3	72.3	105.0
10	U13		20 Bit Buffer	IDT74FCT16827C	TSOP 56	074 x .15	0.650	0.325	24.54	7.43	35.0	38.4	42.9	50.8	53.2	61.2	81.2	105.0
11	U11		18 Bit Register	SCAN18374TSSC	SSOP56	Assumed		0.325	24.54	7.43	35.0	38.4	42.9	53.0	55.4	63.4	83.4	105.0
12	U12		16 Bit Buffer/Driver	SN74ABT16244AI	SSOP 48	057 x .13	0.115	0.115	26.39	9.00	35.0	38.4	42.9	53.4	54.4	57.5	77.5	105.0
13	AR1		Op Amp	CLC412AJE	SOIC 8	039 x 078	1.468	0.300	56.63	30.94	35.0	38.4	42.9	53.5	62.8	79.8	99.8	105.0
	AR2		High Speed Video Op Amp	AD811AR-16	SOIC 16	062 x .098		0.016	28.58	10.25	35.0	38.4	42.9	53.6	53.8	54.3	74.3	105.0
	AR3		Op Amp	CLC412AJE	SOIC 8	039 x 078		0.128	56.63	30.94	35.0	38.4	42.9	53.1	57.1	64.3	84.3	105.0
	AR4		Op Amp	CLC412AJE	SOIC 8	039 x 078		0.128	56.63	30.94	35.0	38.4	42.9	53.5	57.5	64.7	84.7	105.0
	AR5		Op Amp	CLC412AJE	SOIC 8	039 x 078		0.128	56.63	30.94	35.0	38.4	42.9	53.0	57.0	64.2	84.2	105.0
	AR6		High Speed Video Op Amp	AD811AR-16	SOIC 16	062 x .098		0.320	28.58	10.25	35.0	38.4	42.9	53.3	56.5	65.7	85.7	105.0
	AR7		High Speed Video Op Amp	AD811AR-16	SOIC 16	062 x .098		0.320	28.58	10.25	35.0	38.4	42.9	53.6	56.8	66.0	86.0	105.0
	AR8		Op Amp	CLC412AJE	SOIC 8	039 x 078		0.128	56.63	30.94	35.0	38.4	42.9	52.1	56.1	63.3	83.3	105.0
14	G1		Oscillator, CMOS, 5 Mhz	091-9AX	FP 20		0.016	0.003			35.0	38.4	42.9	50.4	50.4	50.4	70.4	105.0
15	G2		Oscillator, Temp compensa	Motorolla	Custom		0.110	0.110			35.0	38.4	42.9	50.9	50.9	50.9	70.9	105.0
17	S1		RF Switch, GaAs SPDT	SW-313	FP 16		0.020	0.010			35.0	38.4	42.9	50.7	50.7	50.7	70.7	105.0
	S2							0.010			35.0	38.4	42.9	52.0	52.0	52.0	72.0	105.0
18	VR1		Dual P.S. Supervisor	TL7770-5QDW	SOP 16	091 x .11	0.025	0.025	50.75	37.17	35.0	38.4	42.9	50.9	51.8	53.1	73.1	105.0
19	VR2		-12V Voltage Regulator	MC79M12BBDT	DPAK	070 x .07	1.830	0.915	13.64	6.37	35.0	38.4	42.9	53.7	59.5	72.0	92.0	105.0
20	VR3		+12V Voltage Regulator	MC78M12BDT	DPAK	056 x .07		0.915	13.64	6.37	35.0	38.4	42.9	53.2	59.0	71.5	91.5	105.0
				Board B Total Power			8.131											

XXX.XXst Component

4.3.4 Software

The on-module software and the majority of test software was developed by the military program. The software task for IBP-MPCL was to determine what software had to be written/changed, and if commercial techniques could be used.

4.3.4.1 On-Module Software Updates

The IBP-MPCL modules required some software changes due to the re-design. The switch from EEPROM memories to FLASH memories, which interface with the DSP ASIC, required a change to eliminate byte writes and to have the page size set to 128 bytes. With the EEPROMs, a page can be from one byte to 256 bytes for the 128k byte version. This affected the boot software loaded on the module. The MTC software remained resident within an EEPROM instead of conversion to flash because this software was not designed by TRW. TRW did not have access to the source code for the software to make change. The on-module test code EEPROM also had changes made to it. Code differences were caused by differences in the SBIT (startup built in test). The remainder of the on-module test software stayed the same.

The software for the Cypress PROMs, which contain sine look-up tables, did not change from the military program. The military controlled software was used as the baseline. The TMS320C31 processor has device test software that was released along with a test specification. The break-up of the DSP MCM moved the testing which was previously done at the MCM level, to the module level. New routines were written to check out the bank of 512kx36 SRAMs, 128kx8 FLASH, the TMS320C31 microprocessor, its interface, and the DSP ASICs interconnect test registers / diagnostics.

4.3.4.2 Software Framework

This section describes the requirements and basic capabilities of the IBP-MPCL software for both the RF/FEC and the PNP modules. The framework used was consistent with the military program, and the documentation of software framework is one of the tasks identified by the software group on the commercial program. Software code was developed consisting of various routines that lead to the successful checkout of each module. The code is developed in a building block fashion so that each routine is run upon successful completion of the previous routine.

4.4 Detailed Design

This section describes the hardware design for both the DV and PV phases of the program. Figures 4.4-1 through 4.4-4 show pictures of both sides of the two modules that were redesigned for the IBP-MPCL program.

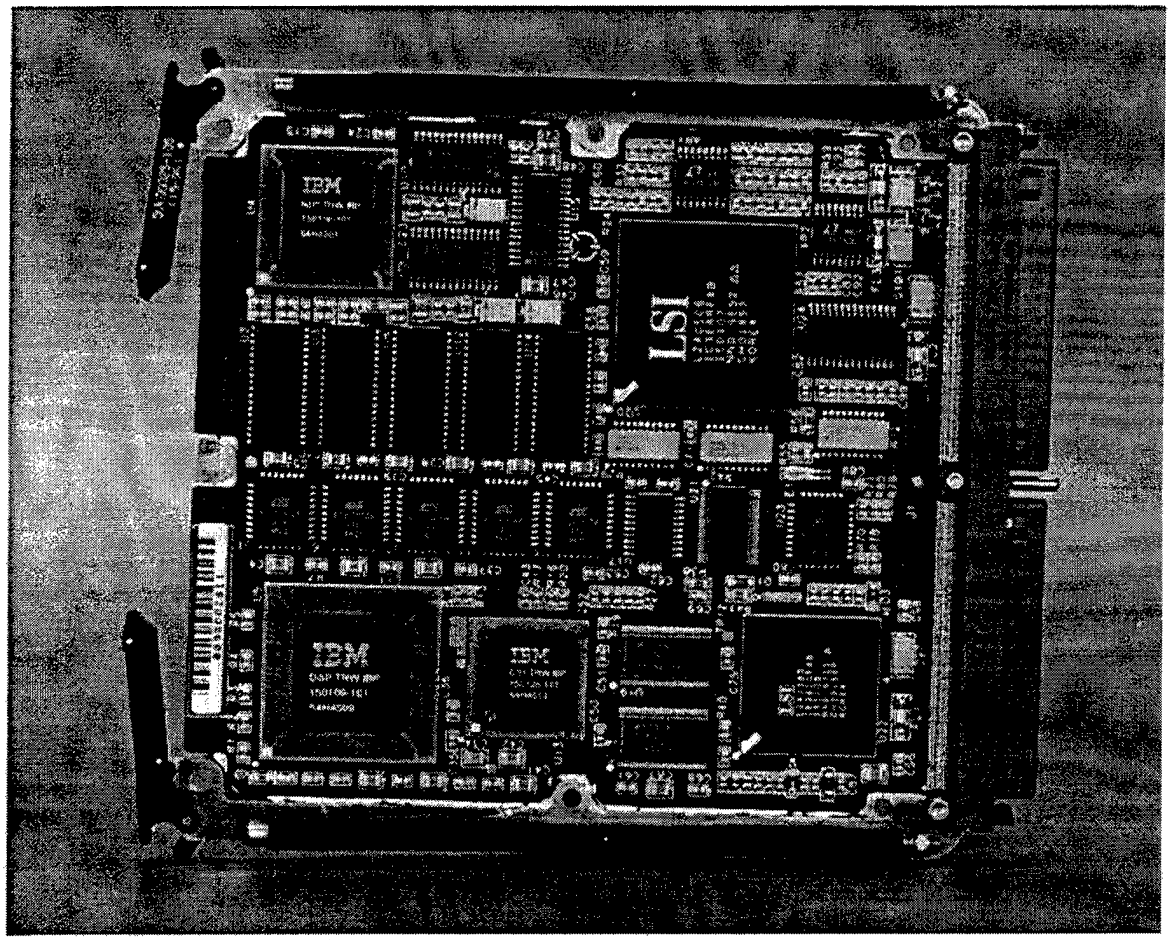


Figure 4.4-1 PNP Module, A-Side View

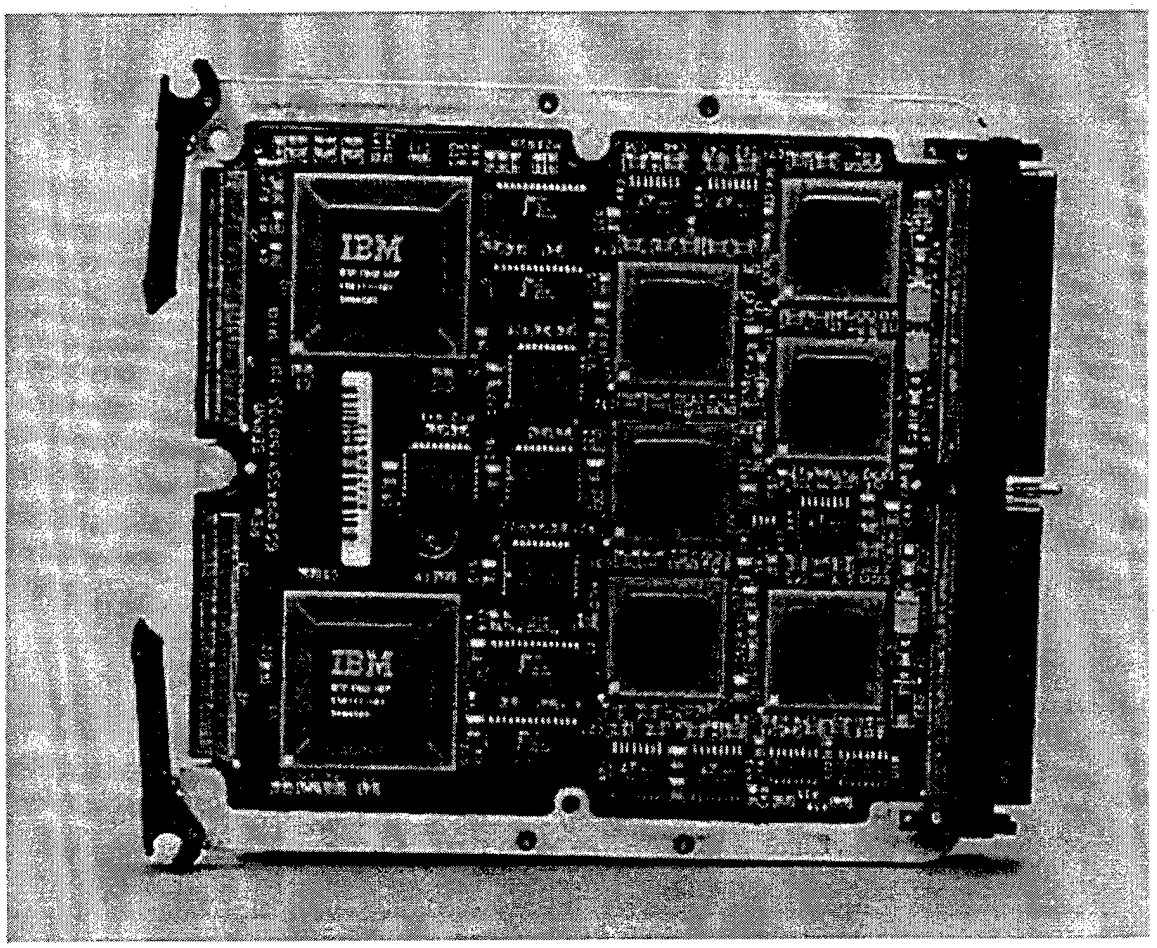


Figure 4.4.2 PNP Module, B-Side View

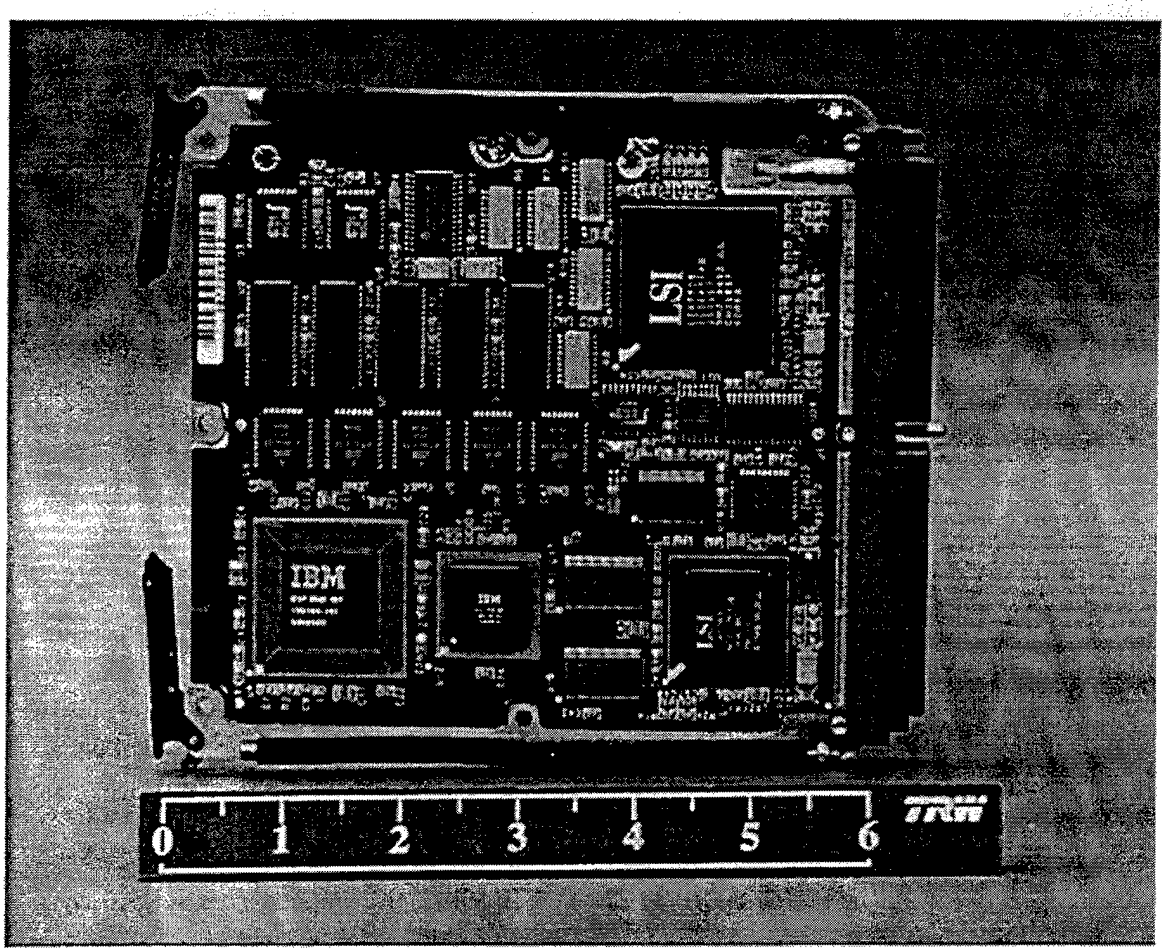


Figure 4.4-3 FEC Module, A-Side View

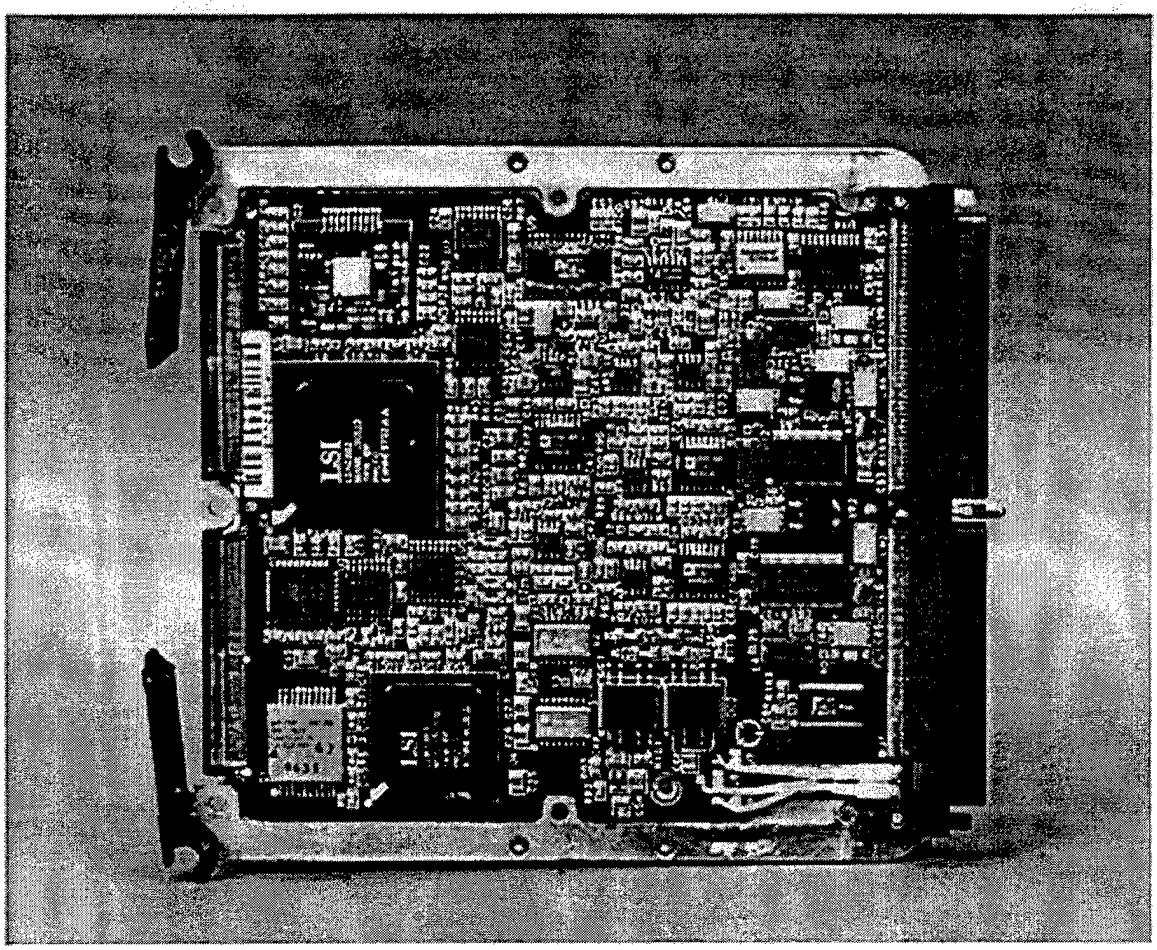


Figure 4.4-4 FEC Module, B-Side View

4.4.1 Electrical Design

4.4.1.1 Printed Circuit Design Rules

Design rules contain information pertaining to physical attributes of the product that affect fabrication, assembly and test. For IBP-MPCL, TRW ASD and TRW AEN design rules were merged. TRW ASD design rules were based on empirical results from low volume manually assembled product. TRW ASD design rules covered fairly complicated real estate limited product. TRW AEN design rules are based on IPC requirements tailored to the automation line for a given product. Automotive product was less IC intensive and dense. To merge these rule sets, the team reviewed each requirement by line, and reconciled differences.

TRW ASD rules were used for printed circuit board densities (lines, spaces, via sizes, drill sizes, routing stay outs, etc.). TRW AEN rules were used for soldering, fixturing and test features (pad size calculations, part to part positioning for automation, card edge stay-outs, tooling holes, fiducials, test point size, test point shape and position). TRW AEN rules were also followed for panelization (size limits, marking, bar code,

fiducials, process patterns). Violations of these rules were identified for process development actions.

The resulting design rules are in use at each facility. TRW AEN used this document as a basis for increased product complexity. TRW ASD has found that the automation assembly rules improve low volume, manual assembly results.

4.4.1.2 Routing Rules

Routing rule documents were created for each of the printed wiring boards. The purpose of a routing rule document was to convey all the routing requirements to board layout personnel. Topics covered by the document are:

- Board stack-up
- Component placement
- Power distribution into the board
- Power splitting on the same plane (where required)
- Critical signal routing – manual routing
- Controlled Impedance layer routing – manual routing
- Routing order for the routing tool
- Rules describing line width and line width
- Rules for parallelism to minimize crosstalk

Routing rules are discussed at a layout kick-off meeting prior to board layout. Routing rules add to the familiarization of the design for the layout people. Reviews are conducted throughout the layout process for adherence to the rules.

4.4.1.3 Schematics and Netlists

Schematics from the military program were copied to a new directory and updated with new components containing AEN part numbers. After the schematics were checked, a Mentor tool was run that packaged the design, and created the netlists. Signal reference sheets, and power ground reference listings were created.

In the netlist each signal name is shown with corresponding connection to the associated reference designator. For example: signal DSPEMUENN goes from U4-AE23 to resistor R25-1, and to U23-4. This output is very useful in checking the IBP-MPCL schematics against the military version. Without a thorough review of this output listing, a signal can be missed. A no-connect on a signal will show up on the netlist as a single connection. On the IBP-MPCL program, all boards were checked to the netlist file prior to fabrication.

A shortcoming of the netlist file is signal naming. For named nets on the schematic it is easy to trace connectivity. For signal traces that were not named by the designer, the

tool assigns an N$1234 number. This is not shown on the schematic, so the N$ trace can be located on any of the schematic sheets. To use the netlist for check, it is best to name as many of the signals as practical. IBP-MPCL named 99% of the nets.

4.4.2 Mechanical

4.4.2.1 Module Covers

The primary requirements for the covers are to protect the electronics from handling, provide Electromagnetic Interference (EMI) protection and identify the product. The DV cover designs are detailed in the drawings: DV150295 - Cover, Side A (PNP), DV150296 - Cover, Side B and DV150297 - Cover, Side A (FEC). The DV covers were designed as a machined aluminum frame bonded to an M55J graphite epoxy web. Because of the mismatch in CTE between the graphite epoxy web (4 ppm/°C) and the aluminum frame (22ppm/°C), a compliant adhesive (Arlon 99510N008) was selected to minimize warping and bondline fracture over temperature extremes. This material is not electrically conductive. In order to insure conductivity for EMI shielding, a bead of conductive adhesive was placed internally around the inside of the cover. The DV covers successfully passed all required testing except for corrosion testing. The web to frame bondline corroded and failed during exposure to the salt atmosphere test. For the PV phase a redesign effort was undertaken.

The PV cover designs are detailed in the drawings: 853547 - Cover, Side A (PNP), 853548 - Cover, Side B and 853567 - Cover, Side A (FEC). The primary difference between the DV design and the PV design was that the PV covers are a one-piece compression molded graphite epoxy structure. The web is a 2-ply high modulus graphite cloth and the frame is co-molded chopped graphite loaded epoxy. The cover was redesigned so that the A and B covers are identical through the initial molding. At the machining step (drilling) the A covers are drilled and countersunk and the B covers are drilled and helicoils are inserted. Final cover differentiation when the silkscreen identification markings are added. This single mold design reduces tooling cost. In order to provide additional shielding for EMI and corrosion protection, the covers are plated with nickel and overplated with cadmium.

The baseline digital module covers were machined Aluminum-Berylium metal matrix (AlBeMet). These redesigns were undertaken to achieve a design that provided adequate component protection from EMI and handling at a lower cost than the military approach. Table 4.4.2.1-1 shows a comparison of material properties.

The cover provides the surface area needed for module identification. The cover is marked with information such as backplane keycode, ESD cautions, and module serialization and revision. The baseline covers have all the product unique data

silkscreened and the serial number unique information ink stamped on at time of manufacturing. For IBP-MPCL, product data was silkscreened but a label was used for serial number unique information and barcoding. The TRW AEN plant prefers labels for product identification on their automotive products. The potential exists to create a label that contains all the product and serial number unique data and eliminate the need for silkscreening covers. Another advantage to this would be the elimination of a part number because both of the "A" side covers would be identical. A picture of the cover is shown in Figure 4.4.2.1-1. The final PV cover designed passed all tests required to validate the hardware.

Table 4.4.2.1-1 Cover Material Property Comparison

Material:	Density: (lb/in^3)	E: (msi)	CTE: (ppm/8C)	K: (W/m-K)
Al (6061)	0.098	10.0	22.5	152
AlBeMet 160	0.076	26	11.4	121
Gr/Ep + Al (approx.)	0.08 (Gr/Ep + Al)	45 (Gr/Ep)	-1.1 (Fiber)	34.6 (Gr/Ep)

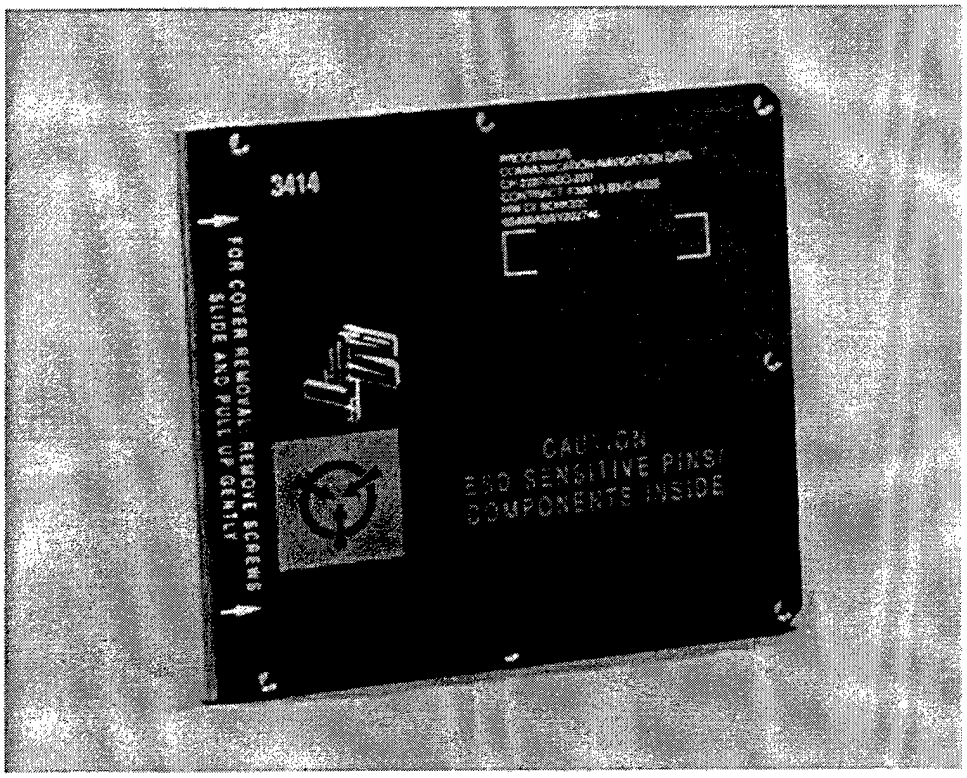


Figure 4.4.2.1-1 IBP-MPCL Module Cover

4.4.2.2 *Thermal Planes*

The thermal planes provide the primary structural support of the modules as well as the path for conducting heat from the electrical components to the integrated avionics rack (IAR) rails. The introduction of plastic encapsulated microcircuits (PEMs) with poor thermal conductivity into the design has created the need for improved thermal conductivity in the core. In addition, with large components with non-compliant attach methods it is important to have a high modulus core that is stiff enough to prevent failure of solder joints in the aircraft vibration environments. The military thermal planes were made from Silicon Carbide Aluminum (SiC/Al). The DV thermal plane designs are detailed in the released drawings: DV150293 - Thermal Plane (PNP), DV150294 - Thermal Plane (FEC). The material chosen was aluminum-infiltrated carbon-carbon. It has a thermal conductivity in the lateral axis approximately twice that of aluminum and stiffness about four times that of aluminum. Additionally, it is about 80% of the density of aluminum and about half the cost of the military core. The coefficient of thermal expansion is much lower than that of circuit components, which requires the use of a compliant adhesive between the boards and the core to decouple the two during thermal expansion.

The aluminum-infiltrated carbon-carbon is made from carbonized preforms that are laid up with woven graphite fibers. The fibers are laid up in a 4:1 ratio with the higher density fibers running in the direction of desired stiffness and thermal conductivity. Aluminum is cast into the preforms which improves the Z axis thermal conductivity and the ability to machine the material. In the casting process, the preforms are slightly smaller than the mold, which results in thin aluminum skins on the part after casting. These skins must be machined off prior to detail machining to prevent warping in the part due to uneven stress distribution. This material selection was not carried over to the PV phase of the program because a plating solution could not be found that provided sufficient corrosion protection.

The PV thermal plane designs are detailed in the released drawings: 853546 - Thermal Plane (PNP), 853566 - Thermal Plane (FEC). The primary difference between the DV and the PV design is the material change to a K13C2U graphite fiber in a cyanate ester resin. The material is layed-up and compression molded to near net shape. The bosses and rail details are machined to the final dimensions. For corrosion protection, the graphite epoxy material is plated with nickel and cadmium. The PV core design passed all tests required to validate the hardware.

Table 4.4.2.2-1 and Figure 4.4.2.2-1 show comparisons of material properties used for thermal planes. Figure 4.4.2.2-2shows a picture of the IBP-MPCL Thermal Plane design.

Table 4.4.2.2-1 Thermal Plane Material Property Comparison

Material:	Density: (lb/in^3)	E: (msi)	CTE: (ppm/8C)	K: (W/m-K)
Al (6061)	0.098	10.0	22.5	152
SiC/Al 70%	0.108	38.4	6.2	170
Al/C-C 4:1	0.0776	42.05	0.0	351
K13C2U	.058	40	-1	290

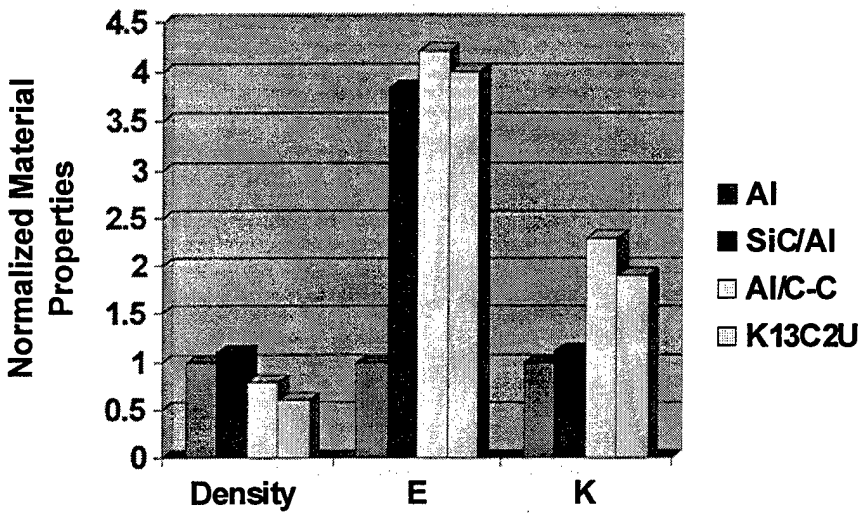


Figure 4.4.2.2-1 Thermal Plane Material Property Comparison

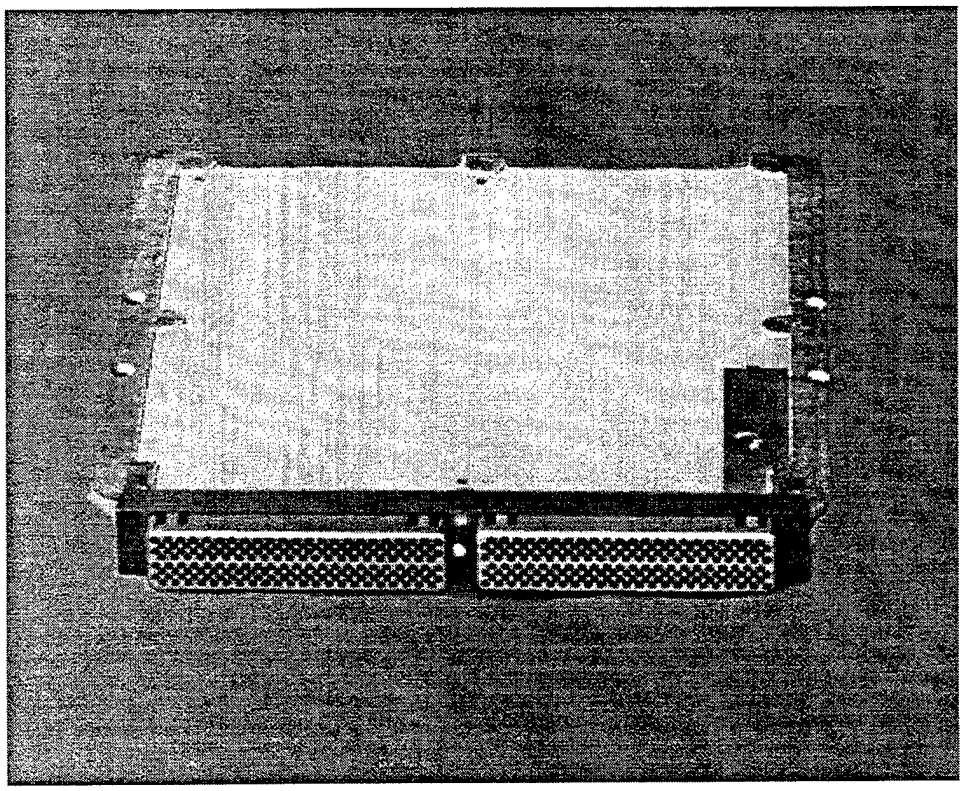


Figure 4.4.2.2-2 IBP-MPCL Module Thermal Plane with Backplane Connector

4.4.2.3 Printed Wiring Boards

4.4.2.3.1 Construction

The printed wiring board designs are detailed in the released drawings: 853552 - Printed Wiring Array PNPA, 853557 - Printed Wiring Array PNPB, 853572 - Printed Wiring Array FECA, 853577 - Printed Wiring Array FECB. The printed wiring boards are constructed from Bismaleimide Triazine/Epoxy (BT/Epoxy) laminate. This material is selected because it is the same material that is used for PBGA substrates and has a glass transition temperature near solder reflow temperature (180°C). This allowed for the best CTE match between the module and critical parts and minimal stress on the PTHs during reflow. Each board is a 0.050 inch thick, 10 layer board with layer stack-up as shown in Table 4.4.2.3.1-1. Minimum allowable line width and spacing are 5 mils. Holes require etchback for 3 point contact and 2 mils of copper plating for durability. Solder mask is dry film conformask to tent the vias (to avoid core bond adhesive seepage and promote vacuum on bed of nails test) and to isolate metal case parts from the PWB traces. Exposed copper is coated with electrodeposited solder 0.3 to 1 mil thick.

Each net has a backside testpoint for in-circuit testing. The boards are built in two-up arrays that conform to AEN standard panel sizes. Arrays are fabricated per IPC A 600 Class 2. Figure 4.4.2.3.1- 1 shows a printed wiring board array.

Table 4.4.2.3.1-1 Printed Wiring Board Layer Stack-up

	PNP-A 853552		PNP-B 853557		FEC-A 853572		FEC-B 853577	
Layer Num	Description	Copper Wt	Description	Copper Wt	Description	Copper Wt	Description	Copper Wt
1	Cmpnt	1/2 oz	Cmpnt	1/2 oz	Cmpnt	1/2 oz	Cmpnt	1/2 oz
2	Ground	1 oz	Ground	1 oz	Ground	1 oz	Ground	1 oz
3	Signal	1/2 oz	Signal	1/2 oz	Signal	1/2 oz	Signal	1/2 oz
4	Signal	1/2 oz	Signal	1/2 oz	Signal	1/2 oz	Power	1 oz
5	Power	2 oz	Power	2 oz	Power	2 oz	Signal	1/2 oz
6	Signal	1/2 oz	Signal	1/2 oz	Signal	1/2 oz	Signal	1/2 oz
7	Signal	1/2 oz	Signal	1/2 oz	Signal	1/2 oz	Ground	1 oz
8	Ground	1 oz	Ground	1 oz	Ground	1 oz	Signal	1/2 oz
9	Signal	1/2 oz	Signal	1/2 oz	Signal	1/2 oz	Power	1 oz
10	Circuit	1/2 oz	Circuit	1/2 oz	Circuit	1/2 oz	Circuit	1/2 oz

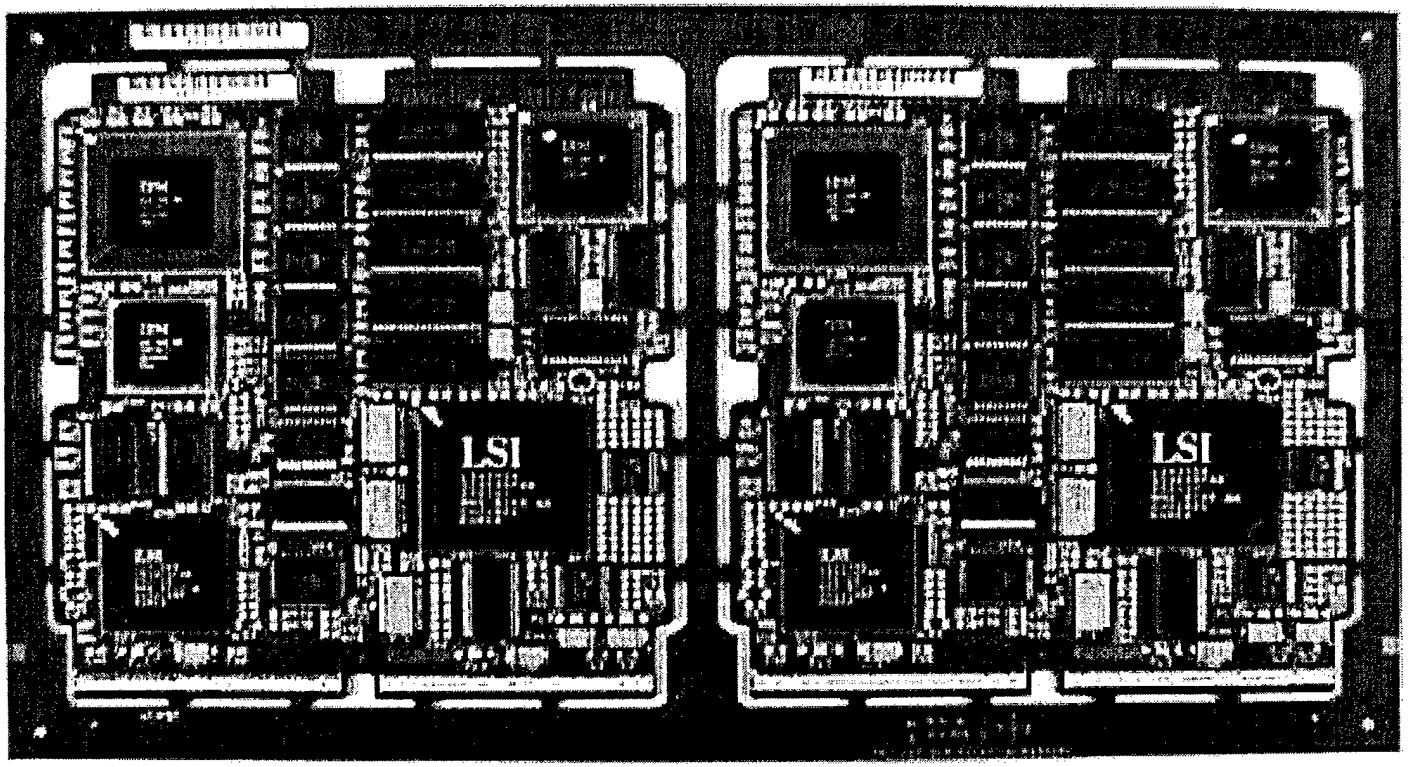


Figure 4.4.2.3.1- 1 Printed Wiring Board Array with Components Assembled

4.4.2.3.2 Layout

The preliminary parts layout was performed using the military board versions as a guide. Many parts were selected in different packages, the functionally equivalent part was placed in a similar location. The layouts on the "A" boards were complicated by the break out of the Multi-Chip Module (MCM) for the DSP ASIC, microprocessor and memories used in the military version. Final layout was determined based on thermal, routing and timing considerations.

4.4.2.4 Parts

All of the ASICs and the C31 μ processor were repackaged in plastic ball grid array packages. Table 4.4.2.4-1 shows the various size ball grid array packages that are on these modules, along with the package supplier. This packaging approach drove material choices to help insure adequate durability. Most of the microcircuits were selected from commercially available plastic encapsulated packages. These replaced the military versions that were in hermetic ceramic leaded packages. The FEC 10 Mhz oscillator was too tall to fit on the military module without a cutout in the board to allow mounting directly to the core plate. An alternate part was selected that would fit in the IBP-MPCL module as a surface mount component. In addition, the military FEC design included a daughter card that fit in a board cutout for mounting op-amp circuits. These were also redesigned to be 100% surface mount.

Table 4.4.2.4-1 PBGA Packages and Suppliers

Part	Die Supplier	Package Style	Size	Use	Package Supplier
DMAD	Maxim	169 Ball, Full Grid	23 mm	PNPB (6)	IBM
C31	TI	169 Ball, Full Grid	23 mm	PNPA, FECA	IBM
MTC	LSI	225 Ball, Full Grid	27 mm	PNPA, FECA, B	LSI
NBP	Motorola	256 Ball, Peripheral Grid	27 mm	PNPA	IBM
MAME	LSI	313 Ball, Staggered Grid	35 mm	FEC B	LSI
CBIU	LSO	313 Ball, Staggered Grid	35 mm	PNPA, FECA	LSI
RTP	Motorola	352 Ball, Peripheral Grid	35 mm	PNPB (2)	IBM
DSP	Motorola	352 Ball, Peripheral Grid	35 mm	PNPA, FECA	IBM

4.4.2.5 Adhesives

4.4.2.5.1 Component

Some of the components require adhesive bonding to the module for either structural or thermal performance.

Components that require adhesive for structural performance fall into one of two categories. They are either large leaded components whose mass would cause large

stresses in the solder joints under vibration loading or components with an irregular lead configuration (i.e., leads on only one side of a package) which could result in asymmetric loading of solder joints. Decisions to bond these parts are primarily based on engineering judgment, in absence of empirical data.

Components require thermal adhesive when the junction temperature is higher than desired. This assessment is based on the module and component thermal analysis. The use of thermal adhesive to ensure lower component junction temperatures enhances reliability, durability and electrical performance.

The material requirements for the bond adhesive are that it have a high thermal conductivity to help cool the parts and a low CTE to prevent loading the component solder joints due to Z axis expansion. Reworkability of the adhesive is an additional desirable characteristic. Beyond these characteristics, the material selection was left to manufacturing to address producibility concerns. The required effective thermal conductivity is 0.024 W/in-C. The effective conductivity is the material thermal conductivity times the percentage coverage under the die. The baseline material chosen for this was Loctite 5404. It has a conductivity of 0.034 W/in-C and therefore, 70% coverage under the die is required to achieve the desired effective conductivity.

4.4.2.5.2 Board to Core

The board to core adhesive provides the structural and thermal interface between the printed wiring board and the thermal plane. Because of the very low coefficient of thermal expansion of the thermal plane, it is required that the adhesive have a very low elastic modulus. This allows the expansion of the board and thermal plane to be decoupled from each other. In addition, the thermal conductivity must be as high as possible to insure good heat conduction to the thermal plane. This adhesive must also be electrically non-conductive to isolate the circuit care test points from the thermal core ground. As with the component adhesives, these performance requirements were given to manufacturing and the final decision on materials was left to address producibility issues. The required effective thermal conductivity is 0.02 W/in-C. The maximum modulus of elasticity is 220 ksi. The baseline material chosen for this was Loctite 5404. Figure 4.4.2.5.2-1 shows the results of CTE testing of a BT/Epoxy boarded bonded with Loctite 5404 to a P120 core. The figure shows that the adhesive effectively decouples the board and core above –33°C. Below this temperature, there is a significant amount of coupling.

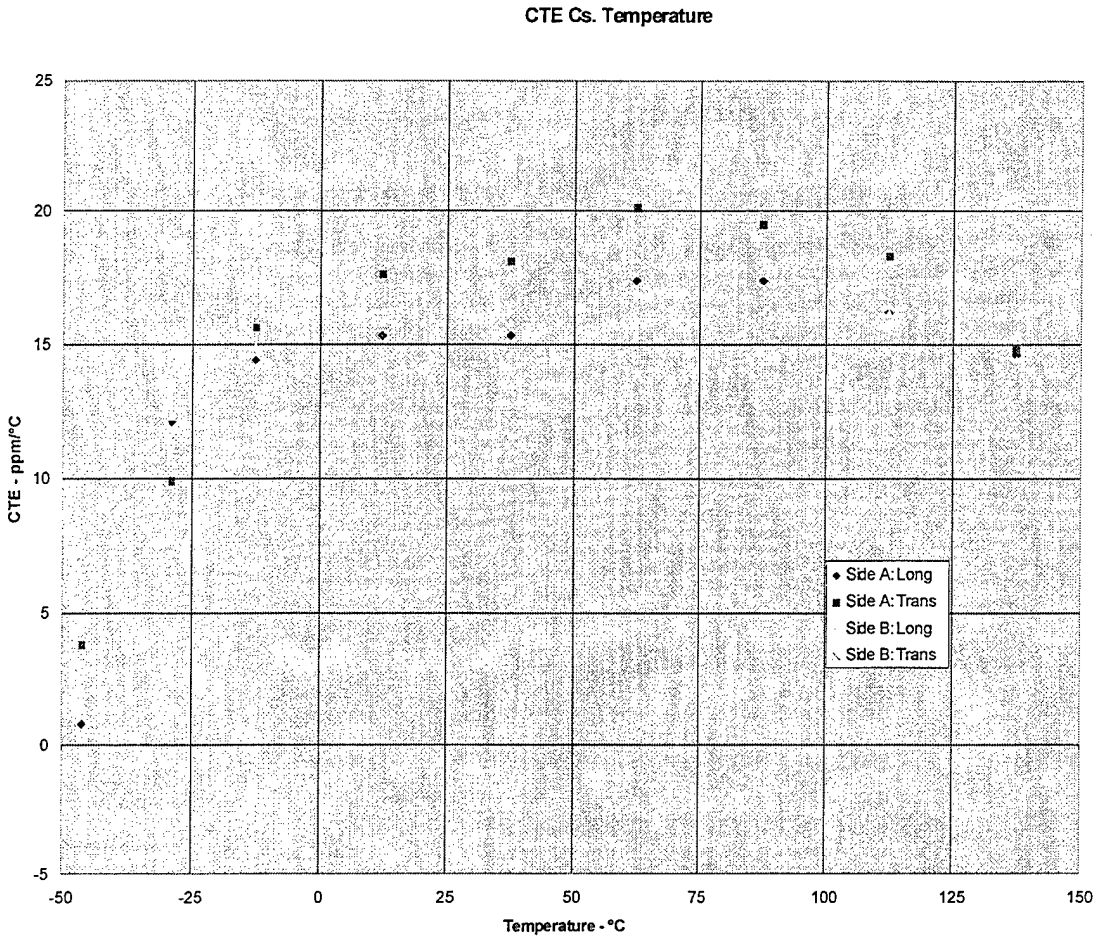


Figure 4.4.2.5-1 CTE Variation with Temperature for Board Bonded to Core

4.4.2.6 Common Components

In order to maintain control of interfaces and due to the desire for commonality, the customer has dictated the procurement of certain hardware for all SEM-E modules. These requirements have followed up by IBP-MPCL. These components include backplane connectors (5VK00065-101, 5VK00065-129), wedgelocks (5VK00026-104) and inserter/ejector levers (5HK01180-103/-104). Figure 4.4.2.6-1 shows some of the common components along with the core and crossovers.

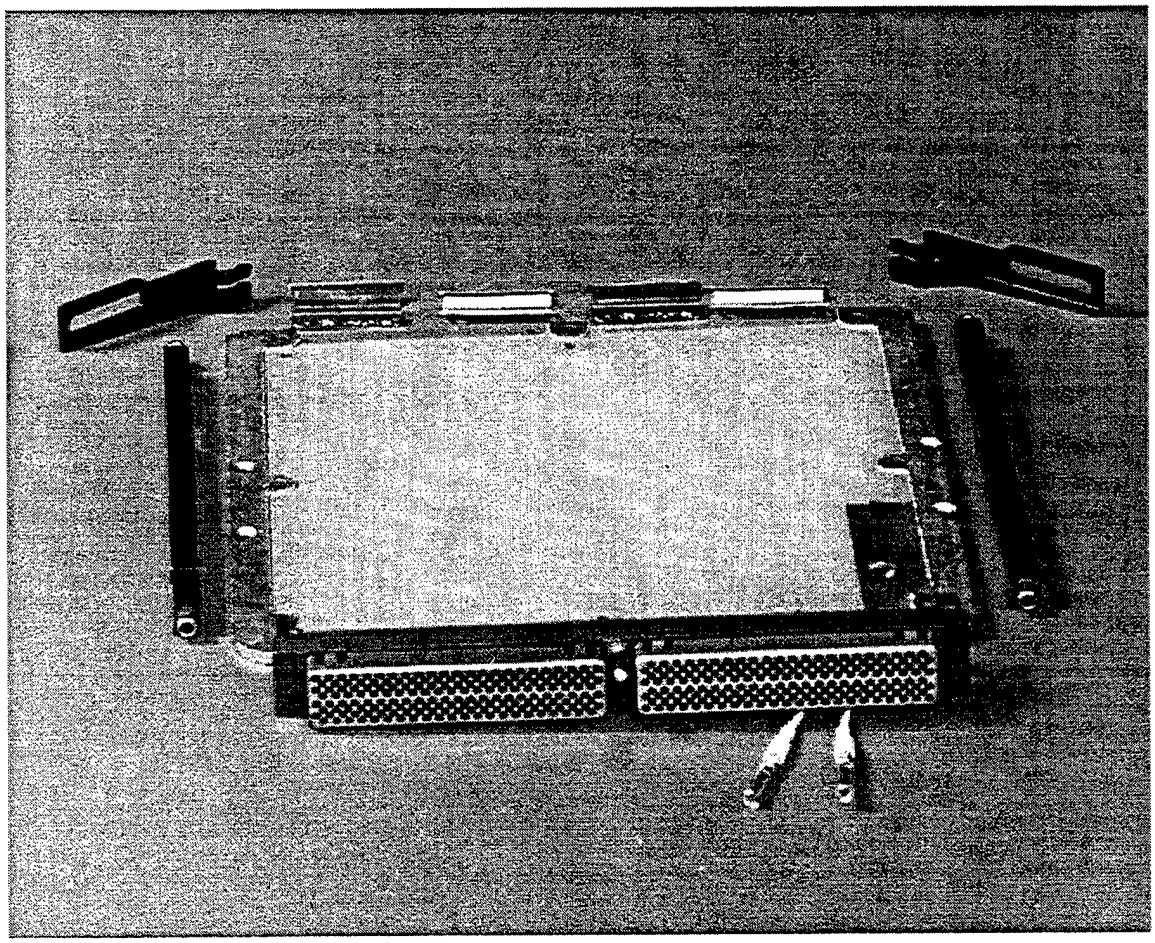


Figure 4.4.2.6-1 Common Components

5.0 MANUFACTURING

Manufacturing processes that were developed related to all aspects of hardware assembly from component level repackaging through circuit card assembly and module assembly. These sections detail the manufacturing process used and developed for the IBP-MPCL program.

5.1 Parts

5.1.1 ASICS

5.1.1.1 IBM ASICs

A contractual agreement was made with IBM Microelectronics to manufacture PBGA packaged, custom devices that had previously existed in hermetic flat-packs. The custom devices were three Motorola H4C ASICs (DSP, RTP, NBP), a Texas Instruments C31 DSP, and a MAXIM Dual Monolithic A-to-D Converter.

Initially, there were a considerable number of contractual hurdles to overcome in order to do business with IBM. The final agreement was to have the IBM Endicott facility manufacture the needed quantities of devices to support the DV and PV builds for the IBP-MPCL program. Normally, IBM manufactures production quantities (> 10,000 per device type) at their Bromont facility.

The Endicott facility is a low volume production facility normally accustomed to engineering development builds. The devices were new to Endicotts' existing process baseline. The initial lots exhibited fairly high manufacturing defect levels.

Table 5.1.1.1-1 describes the processing problems associated with the manufacturing assembly of the devices and the corrective actions taken.

As a result of the improvements and process changes that were implemented at IBM over a 1 _ to 2 year period, the yield increased from 30-40% up to 80-95%. This demonstrated the difficulty in producing small volume custom ASICs at a third party house.

Table 5.1.1.1-1 Summary of IBM PBGA Assembly Issues and Improvements

Trip	DATES	DEVICE BUILDS	ISSUES	ACTIONS
1	Nov/4-6/97	RTP,DSP	Encapsulant defects (bubbles/ microcracks) occurred during CR2 testing and subsequent DV builds.	A slower dispense rate of encapsulant to minimize air entrapment was implemented as well as a closer visual check for bubbles while encapsulant still molten.
			Low DSP and RTP yields due to die metal damage (as verified by the presence of crescent-shaped metal damage).	Program for Camalot was changed to locate off laminate surface during encapsulation. Die mount tool was cleaned and covered with kapton to minimize particulant damage.
2	Dec/16-18/97	DMAD	Low wirebond yields and extensive die surface contamination.	Die mount operation was moved to a controlled area to minimize die surface contamination.
3	Jan/11-16/98	RTP,DMAD	Missing DMAD lot (Fishkill), inconsistent wirebond location, DMAD die chipping during dicing.	A wider saw blade was used and the double street cuts were moved closer together.
4	Jan/25-31/98	DMAD,NBP, DSP	Inconsistent wirebond placement and die metal damage during die mount.	Bonder was found to have damaged wedge also a broken spring was found that controlled the wedge position.
5	Feb/9-13/98	DMAD,DSP, C31	Die metal damage during die mount.	A newer die mount tool with a rubber tip was used, which worked well on all die except the DSPs
			Inconsistent wirebond placement.	It was determined that the stage temperature of the wedgebonder affected the sensitivity of the bond positioning, so an air cooling nozzle was installed to blow across the stage during bonding.
6	Mar/9-13/98	RTP,DSP	DSP die metal damage and part marking process startup.	A new, wider delrin tool was implemented and it was cleaned with IPA every 3 die that were mounted.
7	Mar/30-31/Apr/1-3/98	NBP,C31	Monitor yields and C/A implementation.	Assembly results good....no evidence of recurring problems from previous builds
8	Aug/24-27/98	DMAD,DSP	Monitor yields and C/A implementation with new group of DSPs	Results good.....also wirebonder was allowed to thermally stabilize prior to start of build, which further improved placement consistency.
9	Sept/28-Oct /1/98	DSP	Continue to monitor DSP yield.	Assembly results good....4 die with handling scratches.

5.1.1.2 LSI Logic ASICs

The ASICs from LSI Logic (MAME, CBIU, MTC) were delivered as fully assembled and tested devices in PBGA packages.

In this case, LSI Logic provided generic qualification data to support the specific devices being delivered for the IBP-MPCL program. High temperature operating life (HTOL) data was summarized for the 100K gate technology (MAME, MTC) and 300K gate technology (CBIU).

Generic PBGA packaging tests included biased humidity (+85C/85%RH, 5V, 1000 hours), autoclave (+121C, 15psig, 96hours), and temperature cycling (-55C/+125C, 1000 cycles). LSI yields are unknown to TRW. Significant delays occurred in receipt of their components (14 months).

5.1.2 Lead-forming and Tinning

TRW AEN requires all suppliers to provide components lead formed and tinned. IBP-MPCL was not able to procure all components to this goal. A small quantity of component types (5 of 200) needed lead forming and tinning steps after procurement to make them suitable for automatic placement and solder re-flow processing. Three of the components, a 5 MHz oscillator, a directional coupler, and temperature transducer come in metal-ceramic flat-pack style hermetic packages with gold plated leads exiting horizontally from the package. The leads have to be formed (bent down) in order to make contact to the screened solder paste covered contact pads. The leads were then tinned to enhance re-flow solderability and reduce gold embrittlement. Two other components, a 10 MHz oscillator with castellated contacts, and a RF switch needed only tinning. Parts were bought as one part number, and after lead forming and/or tinning, received a new part number. A third party specializing in such processing performed the forming and tinning.

5.1.3 Tape and Reel

For use in automated printed wiring board assembly, surface mounted components are generally packaged in reels of a range of standard sizes. The automated Flex 3 line at the TRW AEN, Marshall plant requires components to be reeled and placed in feeders on the automatic pick and place machines. In the manufacture of the IBP-MPCL boards, reeled components range from 0805 chips to multi-leaded SOL, SOJ, SOIC, SSOP, PLCC and TSOP packages. Components used in sufficient volume were procured in reels directly from the manufacturer. In some instances, the components were of insufficient volume (50 to 300 pieces) and had to be procured from electronic component distributors. These components were received in bulk or in plastic tubes. A third party provided reeling service. The cost of reeling is about $50, and can add significantly to the cost of a low volume component. One component, a temperature transducer, due to its non-standard shape required a special carrier strip to be tooled at a cost of $1000 dollars. This cost was amortized over 135 components. This additional "reeling" cost for low usage components must be weighed against the cost savings of automated in-line placement versus, for example, manual placement on the line before solder re-flow. IBP-MPCL used the more accurate and mistake-proof automated placement.

The GSM placement machine has a remote automated tray feeder capability (Ramtf). All matrix tray components were loaded from the Ramtf. These included 8 part types of BGAs and 7 part types of leaded and formed components. The availability of the Ramtf tray handler provides added flexibility to automatically handle special or low volume components (such as BGA or the lead-formed specialty packages). Insufficient tray capacity usually requires frequent replenishment. Placing components in trays requires extra care to maintain proper parts orientation. Additional documentation and second person verification were used to mistake proof proper tray loading.

5.2 Product Development at AEN

The methodology TRW Automotive Electronics (AEN) uses to develop new products to customer specifications is called Concurrent Development Process (CDP). CDP combines "bookshelf" designs (product and process concepts that can be utilized to develop new products) with concurrent engineering, design for assembly and manufacturability (DFM). The process is comprised of five stages as follows:

- Business Development,
- Product and Process Design,
- Design Verification (DV),
- Product and Process Validation (PV),
- Product Launch / Start of Production (SOP)

Cross-functional product development teams carry out the work in each of the stages under the guidance of a program manager. Product and process engineering personnel from the facility producing the product are involved in all stages of the development. Involvement by plant personnel increases significantly during the last three stages. Product launch is essentially carried out by the plant. At the end of each phase of the CDP process, a phase exit readiness assessment is conducted. This assessment leads the product development team through a disciplined, thorough, and realistic evaluation of the project's readiness to proceed to the next phase of the development process.

There is significant similarity between the standard TRW AEN CDP process and the IBP-MPCL program to develop the PNP and FEC modules. AEN personnel have worked as members of the MPCL process technology (PT) team to provide input to board layout for manufacturability at the Marshall plant. AEN also provided about fifty (50) per cent of the commercial components on the bill of material (BOM) from the AEN component library and helped identify others.

AEN process personnel gained valuable preliminary process experience by building 65 circuit board assemblies at the Marshall facility for CR #1 tests and an additional 20

assemblies for CR #2 component reliability testing. These builds provided first hand experience to evaluate existing processes for placing and reflow soldering new components (such as fine pitch and BGA devices), and provided input to an assessment for the need of additional process improvements.

5.3 Business Plan

5.3.1 Business Strategy

One purpose of the IBP-MPCL program is to test the feasibility of building military hardware on commercial lines, while still meeting military requirements. The objective is to cut costs by using commercial standards and components, as well as identify ways to build up the commercial base in the U.S. for manufacturing military products. As part of the business development phase of TRW AEN's product development, AEN rationalized its participation in this program as an opportunity to evaluate the "dual-use" capability of its commercial processes to manufacturing military products and to identify needed capabilities, if any. Such dual-use capability requires the ability to perform a quick changeover between commercial and military products so as not to affect commercial throughput and capacity. A financial analysis based on ROAE (Return on Assets Employed methodology) was also performed and showed that military modules such as PNP and FEC could be made profitably in AEN's commercial environment.

As a consequence of demonstrating the manufacture of the PNP and FEC modules, AEN gained advanced process technology, acquired new infrastructure including quick changeover capability, and has substantially increased its business potential for manufacturing military hardware.

Another result from this effort is a partnership between TRW AEN and TRW ASD to manufacture CNI modules. Such business is planned to be contracted under new acquisition reform guidelines (See IBP-MPCL Business Practices Manual).

5.3.2 Base Line Situation

During Phase 2, the TRW AEN Marshall IBP-MPCL process team had the responsibility to identify existing processes or develop new ones for manufacturing the PNP and FEC modules. An assessment of the existing processes and resources during Phase 1 applicable to module manufacturing is shown in Figure 5.3.2-1 below. The identified gaps were closed during Phase 2 and early Phase 3 prior to production validation (PV) builds.

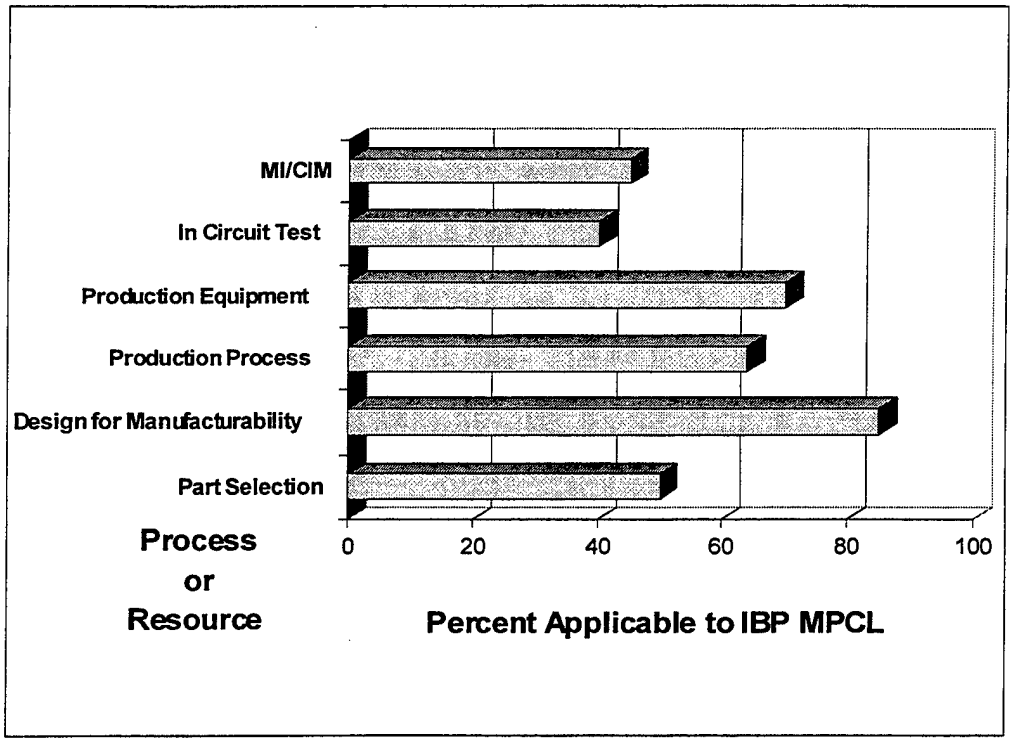


Figure 5.3.2-1 AEN Resources and Processes for Module Manufacturing

During Phase 2, AEN provided design for manufacture (DFM) inputs for lay out of the four boards that go into the PNP and FEC module assemblies. The intent of these inputs was to make the board design consistent with automated factory processes as well as ensure manufacturability to the highest quality levels.

The computer integrated manufacturing system (CIM) in the plant required upgrades which were identified in Phase 1 and 2 and implemented for Phase 3. The new IBP-MPCL CIM system provides for the following capabilities:

- Facilitates design data transfer for manufacturing processes from the ASD design center.
- Facilitates faster manufacturing line changeover for dual-use (commercial /military).
- Improves data collection, accuracy, trending and archiving.
- Establishment of a "paperless" factory by having all information available online at production stations.

Capital improvements were made in Phases 2 and 3 to implement the new CIM system.

The AEN Marshall facility has seven manufacturing lines for manufacturing circuit board assemblies and products. Flex Line 3 was selected during Phase 2 for the PNP

and FEC module boards, since this line represented the best match to IBP-MPCL requirements. It is a medium to low volume, highly flexible line. Circuit boards for sixteen (16) product family groups, with two to twenty variations each are built on this line. Typical volume is 200 panels (a panel contains one or more circuit boards) per shift with several line changeovers. The product mix requires components from 0805s to tantalum D passive components, and active components with 8 to 84 leads on 25 to 50 mil spacing.

Existing in-line equipment to support the range of commercial products consisted of:

- Solder screen printer capable of printing 25 mil spacing
- Turret style twelve (12) head, five (5) nozzle per head, high speed placement machine capable of placing 25 mil devices with 150 feeder storage capacity
- Overhead X-Y gantry style placement system with the ability to place 12 mil devices with feeder and matrix tray capability.

A fully programmable eleven (11) zone top and bottom forced air convection oven is in place for solder reflow. Additional equipment for bottom side and through-hole component placement is available on Flex 3 but is not required by PNP and FEC printed board assemblies. Flex 3 board wash equipment and in-circuit test equipment are used, but commercial module assembly stations were not applicable.

The commercial products built on the Flex-3 assembly line, did not require ball grid array (BGA) components, fine pitch lead components, printed circuit board bonding to thermal cores, or top side adhesive dispensing. There was also a feeder capacity limitation on the total number of different components that could be placed by the line, which would be exceeded by the additional new components needed by the PNP and FEC board assemblies.

5.3.3 Proposed Method

An analysis of Flex Line 3 in-place capabilities indicated that the following processes needed development to support the addition of PNP and FEC board assembly manufacturing:

- Fine pitch (10-mil) solder paste screening
- In-line top side adhesive dispense prior to reflow
- Fine pitch placement and reflow (20 mil lead pitch)
- Ball Grid Array (BGA) placement, reflow, and rework
- In-circuit test of BGA ASICs using boundary scan

- Core bond thermal adhesive, select, develop application and cure
- Hot-bar soldering of connectors and crossover connectors
- Final mechanical assembly

These improvements were implemented with capital upgrades during late Phase 2 and brought on-line in early Phase 3.

5.3.4 Capital Upgrades

Table 5.3.4-1 lists the equipment procured to enhance Flex 3 and to enable this line to successfully manufacture military PNP and FEC boards and modules.

Table 5.3.4 -1 New Capital Equipment on Flex-3

Capital Equipment	New Capability	Cost, $
MPM UP 3000 Fine Pitch Screen Printer	Fine pitch solder paste printing to 10 mils	314,000
Camalot Adhesive dispenser	Precision adhesive dispense	79,600
Panasonic MPA chip placement	Increase line capacity and changeover	198,300
Feeder Additions	Reduce changeover setup time	45,500
Manual Screen Printer	Screen adhesive to the backside of PNP & FEC boards	10,000
Cencorp Router	Increased throughput and mistake proofing	72,000
ToddCo Hotbar station	Add hotbar soldering capability	19,000
SRT 2000 Rework Station	Add capability to rework BGA devices	88,000
Dry nitrogen storage for components on feeders	Store moisture sensitive plastic encapsulated components	15,900
Work tables	Work cell for final module assembly	10,000
Mountz Torque Driver	Low Torque Control	15,000
CIM upgrades	Improved line changeover and data collection	133,000

5.3.5 Acquisition Process, Source of Funds

AEN Marshall plant manufacturing and process engineering prepared a Capital Equipment Appropriation (CEA) to appropriate the funds for the equipment listed in Table 5.3.4 -1. This CEA justified the funds on the business case strategy discussed

above. The actual funds, however, came from the TRW ASD capital budget and not the Marshall plant (commercial) capital budget under a "memo of understanding". In this agreement, Marshall will retain and depreciate the equipment useful for "dual-use" manufacturing. Equipment that is military unique may be returned to ASD for disposal. The equipment was procured and placed on-line by AEN Marshall plant manufacturing and process engineering during late Phase 2 and early Phase 3. All equipment was operational for production validation (PV) builds.

5.4 Production Process Development

5.4.1 Overview

The DV process flow to manufacture the boards and assemble the PNP and FEC modules, was modified before PV builds began. These modifications include individual process improvements based on experience from the DV builds. They also include changes in process flow step numbering. Renumbering was necessary due to a plant wide effort to standardize process numbering and the need for this program to be consistent with this renumbering, since common commercial process steps were to be used.

5.4.1.1 PV Process Flow

Figure 5.4.1.1-1 is the process flowchart that documents the flow implemented and used for the production of all PV level board assemblies and modules. An overview description of this flow and how it uses production equipment on the floor follows:

Moisture sensitive components are stored off-line in a dry nitrogen storage chamber; non-sensitive components are stored in material areas next to the line. Referring to the flow chart, operation numbers (OP #s) 90 through 135, which assemble components to boards and solder re-flow them, are performed on a single in-line section of the topside portion of Flex 3. (See Figure 5.4.1.1-2 for the dual use production equipment floor plan and Figure 5.4.1.1-3 for the "topside" portion Flex 3.) Aqueous cleaning (OP #330, #437 and #587) and ICT test (OP #430) are Flex 3 processes but located further down the line. PCB Singulation (OP #420) is co-located with Flex 4. X-ray (OP #376) is performed on a sample basis on equipment in the Quality Assurance Laboratory. All the equipment and processes described thus far are dual-use with commercial production except OP #115. OP #s 442 through 582 include core bonding and module assembly and are done in a dedicated L-shaped cell area. (See Figure 5.4.1.1-4, Final Assembly Area.) Assembled modules are first sent (OP # 730) to ASD for a sequence of complex functional ATP and ESS tests (OP # 952 to 983). Rework operations can be performed on-line (OP#135) or offline in the final assembly area (OP #136), or at ASD

(OP #957). Upon passing test, modules are returned to AEN for conformal coating (OP # 591 through 597). Conformally coated modules are returned to ASD (OP #990) for final ATP testing (OP #984). This flow could be modified to coat prior to shipment after demonstration of high product yields at test.

Operations where bar code scanning (for CIM system prior step verification) is required or where data collection or SPC occurs are identified with special symbols in Figure 5.4.1.1-1. CIM system work cell controller (WCC) locations, where bar code scanning occurs, are shown on the flow floor plan in Figure 5.4.1.1-2.

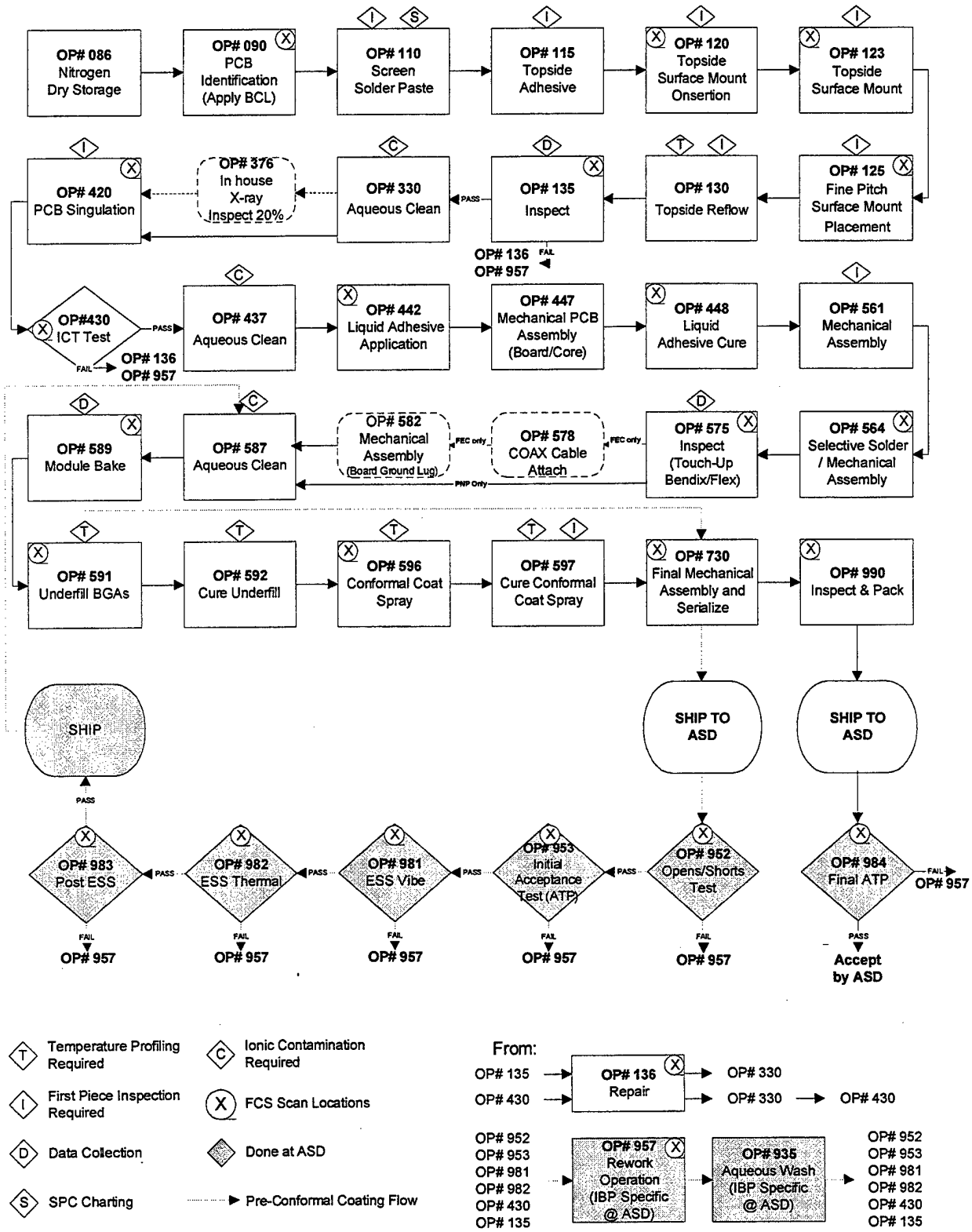


Figure 5.4.1.1-1 PV Process Flow for PNP and FEC Modules

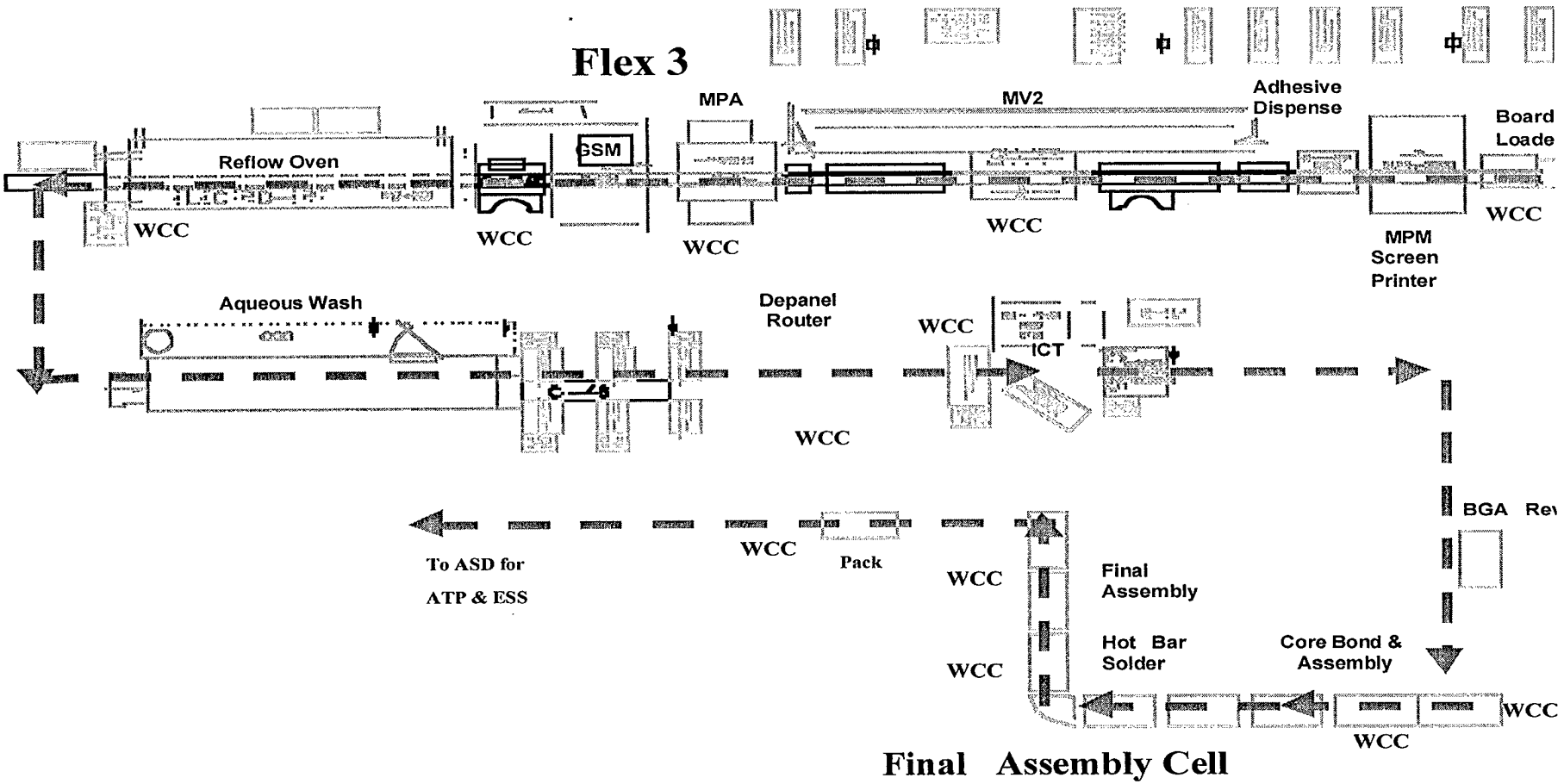


Figure 5.4.1.1-2 Process Flow through Dual-Use Production and Final Assembly Flow

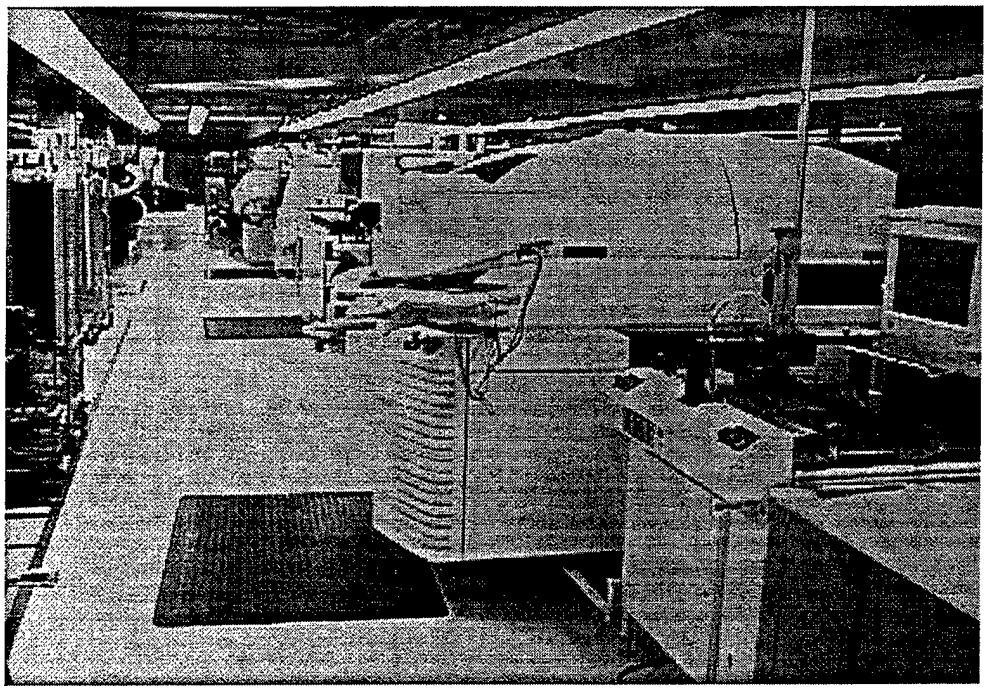


Figure 5.4.1.1-3 Flex 3 Topside Assembly Line

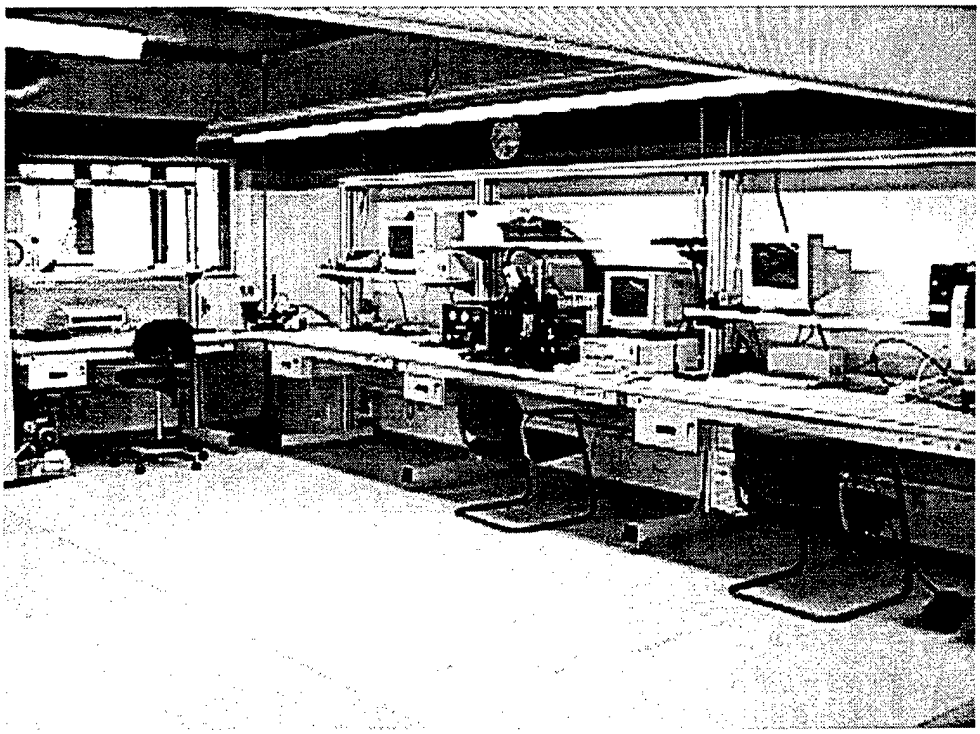


Figure 5.4.1.1-4 Final Assembly Area

5.4.1.2 *Quality Planning*

AEN applied a number of quality planning tools to the process development and manufacture of the PNP and FEC modules. These tools included Process Failure Modes Effect Analysis (PFMEA), a Control Plan, and Quality Model analysis. These tools were initiated during Phase 2 to analyze and improve processes for PV in Phase 3.

5.4.1.2.1 PFMEA

Process failure modes and effects analysis was performed by the IBP-MPCL PT team, which included members from both the ASD and AEN, Marshall facilities. The PFMEA is based on methodology developed by the Automotive Industry Action Group (AIAG). It is a required AEN document for PV builds. The PFMEA analyzes each process step, identifying potential failure modes, potential causes for these failure modes, and process controls in place to prevent them from happening. Ratings are assigned for severity, occurrence, and detection to determine a risk priority number (RPN). High RPN numbers, typically over 100, require improvement action to reduce the RPN. Prior to production example action items resulting from the PFMEA analysis and implemented are shown in Table 5.4.1.2.1-1 below.

Table 5.4.1.2.1-1 Improvement Action from PFMEA for PNP and FEC Module

OP #	Process Name	Potential Failure	Original RPN	Recommended Action	New RPN
090	Bake components	No Bake	168	Use N2 Storage	48
110	Screen print solder paste	Wrong paste	147	Bar code, scan paste with CIM	84
125	Active Component placement	Improperly loaded parts in Ramtf matrix tray	126	First and last piece inspection Visual aids	72
204	CenCorp PCB Singulation	Wrong program loaded	126	Add bar code ID to panel fixture	18

5.4.1.2.2 Control Plan

A Control Plan was also prepared for the process flow outlined in Figure 5.4.1.1-1. It is a required AEN document for products going into PV. The purpose of the control plan is to promote the manufacture of quality products to customer requirements. The plan specifies process monitoring and data collection for key process characteristics, and the reaction plan to be followed when process characteristics are out of control.

Figure 5.4.1.2.2-1 shows the cover page (1 of 6) for the control plan for PNP and FEC modules, including control activities for processes for the first three operations of the process flow chart in Figure 5.4.1.1-1.

CONTROL PLAN

[ ] Prototype [ ] Pre-launch [ ] Production Control Plan Number 0401060	Key Contact/Phone Ron Hill 217 826-2311 Ext 2250 Len Groth 217 826-2311 Ext 2455	Date (Orig.) MAY 8, 1998 ERA# 950444	Date (Rev) Dec 9, 1998 Rev: C ICN# I3835
Part Number/Latest Change Level 202746-1, (PNP); 202747-1 (FEC)	Core Team Ron Hill , Len Groth, Allen Kerr, John Van Sandt	Customer Engineering Approval/Date (If Req'd)	
Part Name/Description LRM PNP Module, LRM FEC Module	Supplier/Plant Approval/Date	Customer Quality Approval/Date (If Req'd.)	
Supplier/Plant TRW Automotive Electronics North America 902 S. Second Street, Marshall, IL 62441 Supplier Code	Other Approval/Date (If Req'd.)	Other Approval/Date (If Req'd.)	

Part/ Process Number	Process Name/ Operation Description	Machine, Device, Fixtures, Tools for Mfg.	Characteristics			Special Char. Class.	Methods					Reaction Plan
			No.	Product	Process		Product/Process specification/ Tolerance	Evaluation/ Measurement Technique	Sample Size	Sample Freq.	Control Method	
086	Nitrogen Dry Storage	Terra Universal N2 Cabinet DS001		Identified Components needing low humidity storage	Relative Humidity in storage unit		<5 % Relative Humidity	Monitor		Continuous Monitoring	Automated	Stop Process and call Product Eng
090	PCB Identification Print, Apply BCL and Load PCB	Intermec Label Printer		Correct Label Stock	Correct Printer Setup		Per Process Instruction	Visual		Each roll	Visual	Stop Process and Re-verify
				Clearly Printed Label	Correct Printer Setup		Readable Text Print	Visual	100%	100%	Visual	Stop Process and Repeat Setup
				Label Location Correct Bar Code Correct Board orientation	Correct Printer Setup Board Placement Operator Label Placement CIM system Setup		Label Suffix and Location on PCB per Process Instructions Machine Readable Bar Code Print	Visual Verification, CIM system bar code reader verification	100%	100%	Visual Verification Location and suffix per Process Instruction. CIM system for Suffix	Stop Process and Correct Bar Cod Setup if required Verify CIM Setu
110	Screen Solder Paste	SSP009 MPM UP 3000 Screen Printer		Solder Paste Registration and Paste Height	Machine Setup		Setup per Process Instruction and Operations Manual	Visual	>1 piece	Start of shift, Product Changeover /Machine Maintenance	Process / Mfg. Instructions	Complete Setup and Re-verify
					Apply Solder Paste to PCB		Solder Paste Coverage Min. 70% Coverage of Pad	2D auto inspection	5 locations on each PCB/Panel	Each Panel	Automated	Shut down until Root Cause is found and Proce in Control
		Cyber Optic LSM01					Solder Paste Height 0.008" ± 0.002" of Stencil Thickness	Cyber Optic Measuring System	5 Locations on each PCB/Panel	Start of Shift, Product Changeover, Machine Maint.	X-bar / R Chart	Shut down until Root Cause is found and Proce in Control
					Auto Stencil Height		Clean Underside of Stencil	Auto Verify	1st Pass	Every 3rd Panel	Auto /Visual	Enable Stencil Wipe
					Solder Paste Age Control		Paste must no equal or exceed expiration date on tube	Visual Inspection	100%	Every Tube	100% Visual Inspection	Scrap any Paste violating Expiration Date. Contact Material Control
					Solder Paste Stabilization		Solder Paste to Room Temperature 7 Days>time>8 hrs.	Tag Solder Paste Tube	100%	All Tubes	Visual	Shut down until paste is within Spec.

Figure 5.4.1.2.2-1 Control Plan Page for PNP and FEC Modules

5.4.1.2.3 Quality Model

AEN Marshall has developed the concept of the Quality Model in order to measure, predict and identify opportunities to improve the quality level of its manufactured products. The Quality Model methodology was applied to the PNP and FEC modules. The primary metric for the Quality Model is parts per million (PPM). The PPM metric is defined as the number of non-conformities divided by board assemblies produced times one million.

The Quality Model breaks down quality information into four areas, namely supplier quality, process quality, design quality, and verification effectiveness as follows:

- Supplier Quality: For the present analysis, supplier quality includes all non-conformities that are dependent primarily on part number and was obtained from the actual component suppliers.
- Process Quality: Process quality is dependent on process and package type. Data from existing lines and equipment was used for IBP-MPCL modules.
- Design Quality: Design quality issues are those due to a non-robust design. It was not considered for the IBP-MPCL modules in this analysis due to design inflexibilities for form, fit and function for military application.
- Verification effectiveness: Verification effectiveness is the measurement of inspection and testing efforts. Verification effectiveness is measured in percent. For example, an in-circuit tester is 90% effective if it detects only 90 % of the defects of a resistor with 100 PPM defect level. Ninety (90) PPM is detected; ten (10) PPM is undetected.

In summary, the Quality Model predicts the quality level of the PNP and FEC modules by summing the non-conformities of the supplied components and processes stated in PPM and modifying these by the verification effectiveness. For the two modules, verification effectiveness relies on visual inspections and in-circuit testing. No final testing of modules is planned at TRW AEN due to the complexity of the testing and the expense of the equipment. Consequently, the PPM level of these models is much higher than typical Marshall commercial product which undergoes extensive final testing.

This analysis predicts the quality level of modules without final testing as follows:

Item	Quality Level in PPM after Verification
PNP A Components	7,097
PNP B Components	9,079
PNP Assembly	9,095
PNP Total	**25,272**
FEC A Components	5,547
FEC B Components	5,071
FEC Assembly	13,818
FEC Total	**24,436**

Section 5.4.4 discusses PNP and FEC module results from PV builds and compares them to this analysis.

5.4.2 Printed Wire Board (PWB) Assembly Processing

The following sections describe in detail the updates of the various processes for building the PNP and FEC printed wiring assemblies (PWB) and modules from DV to PV level and results obtained or lessons learned.

5.4.2.1 Component Handling

5.4.2.1.1 Dry Nitrogen Storage for Active Components (OP #086)

The presence of moisture in plastic encapsulated components must be controlled to prevent cracking in the plastic molded package or internal delamination during the rapid high temperature solder reflow process. Plastic components used for automotive production at the Marshall plant are received in moisture proof packaging. Once removed from such packaging, typical throughput on the floor is high enough that components are consumed (go through solder reflow) before significant moisture re-absorption. Due to low volume requirements, components used in the PNP and FEC modules were obtained from distributors or tape and reeled by third party suppliers during which time their exposure to moisture is uncontrolled. During DV, such components were baked out while in reels and on feeders. The bake cycle used before each DV build, was 40°C for 168 hours to prevent damage to reels.

Figure 5.4.2.1.1-1 provides the recommended time-temperature combinations for component dry-bake prior to reflow solder attach. The higher temperatures may be used if either the devices are baked outside their low temperature packing containers or the packing containers are able to withstand the elevated bake temperatures.

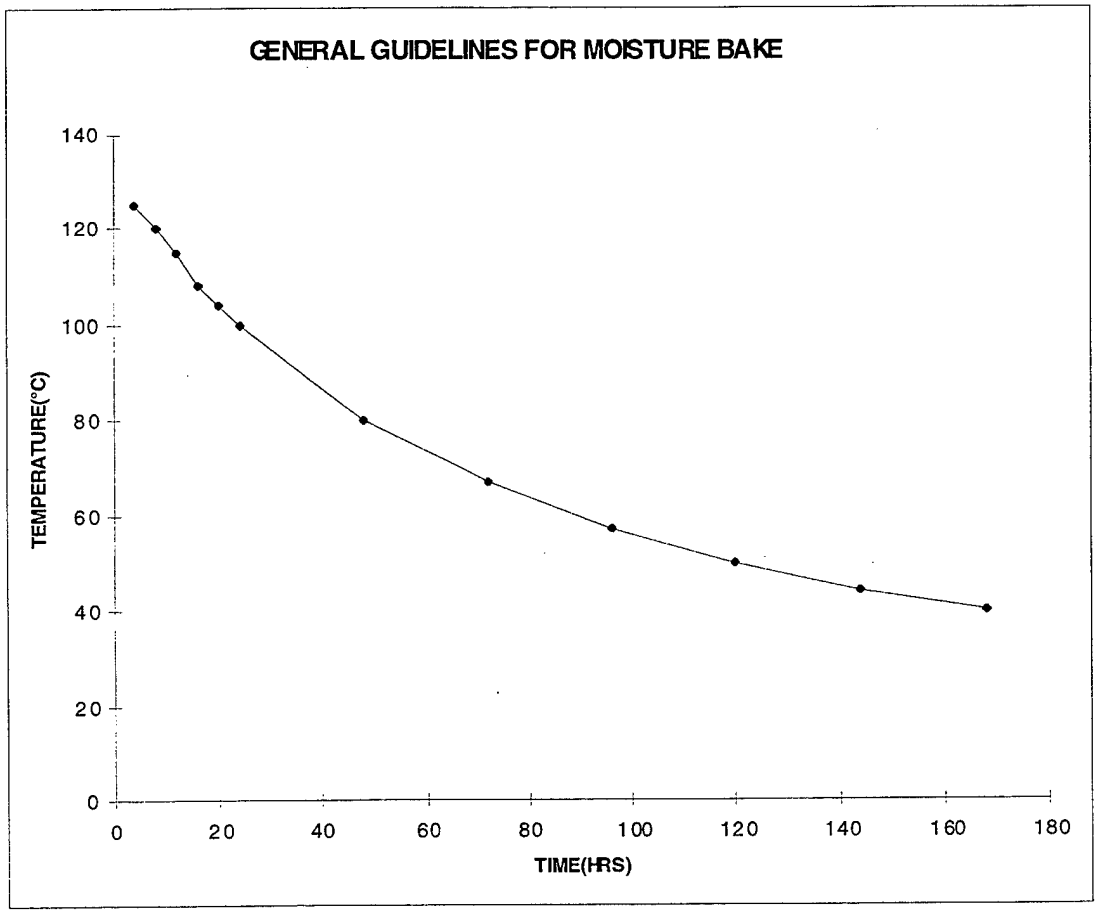


Figure 5.4.2.1.1-1 Recommended Time-Temperature Profile for Plastic Component Dry Bake

This 7-day bake out is inefficient and inflexible. A dry nitrogen storage cabinet large enough to hold all the feeders for moisture sensitive parts was installed. The cabinet maintained an environment of less than five (5) per cent relative humidity. Reeled components on feeders were kept here until needed for setup on the placement equipment. After completion of a build, feeders were returned to this environment. All SOP, SOJ, SOIC, SSOP, PLCC and TSOP and BGA plastic encapsulated components were stored this way.

The component floor life can be defined as the time period which begins after moisture-sensitive devices are removed from moisture barrier bag or controlled storage environments to the time when the devices have absorbed enough moisture to be susceptible to damage during reflow.

Table 5.4.2.1.1-1 shows the classification and floor life of dry packed or dry stored plastic components. The classification is typically specified by the manufacturer on the packing container for the device.

Table 5.4.2.1.1-1 Plastic Component Floor Life Classifications

CLASSIFICATION LEVEL	COMPONENT FLOOR LIFE
1	Unlimited at <85% RH
2	1 year at <30C/60%RH
3	1week at <30C/60%RH
4	72 hours at <30C/60%RH
5	24 or 48 hours at <30C/60%RH
6	Mandatory bake prior to reflow

To date no defective components are attributable to improper storage environment. All non-moisture sensitive parts were stored near the line in the normal factory floor or warehouse environment.

5.4.2.1.2 PCB and Material Identification (OP #090)

Material is tracked in the AEN Marshall facility using bar codes. All direct material issued to the floor has a material tag with part and lot sequence number for material traceablility. When a feeder with a reel is mounted on a placement machine, this material bar code is scanned to a feeder location on the machine. This data is stored in the CIM system database.

PNP and FEC boards were assembled in panels, two boards per panel. A bar code label serialization was attached to each panel and each board on the panel. This ten digit bar code consists of a four digit Julian date (day and year), a four digit serial number, and a two digit product specific alphanumeric suffix. Panel and board labels are 0.25 by 1.5 inches and contain scanable and human readable code. Panel bar codes are in the same location on all panels to be readable by the fixed location scanners on the Flex 3 conveyor. Board bar code location varies depending on board layout. During assembly on Flex 3, the panel bar code is scanned at processes per the flowchart. Direct material information (lot sequence numbers) is automatically assigned to the panel bar code. The CIM system also keeps track of the three bar code numbers from the panel and the two boards in the panel. Scanning a panel bar code at this operation at the beginning of a build tells the CIM system the type of board to be run, and sets up the component machines accordingly.

The panel bar code is discarded, at de-panel and the board bar codes are scanned at the work cells as identified on the Process Flow Chart (See Figure5.4.1.1-1). The CIM system monitors processing steps sequence (prior step verification), so a part cannot be scanned into a process location if the prior step has not passed. At OP #730, the two

boards constituting the module are scanned and the CIM system assigns a module bar code number. All CIM data (date code, material sequence number, quality information) can be accessed under the board bar code number and under the module bar code number.

5.4.2.2 Screen Print Solder Paste (OP #110)

In this operation solder paste is applied simultaneously to the two printed circuit boards in the panel by means of a stencil mounted in a "screen printer". The stencil, typically made of thin stainless steel sheet is mounted on a frame, which installs into the screen printer. The stencil has precision apertures cut into it corresponding to the pad areas on the boards where solder paste is required for re-flow solder component attachment. Solder paste is forced through the apertures by a squeegee blade whose speed and pressure is regulated. Pattern recognition capability is used to align the stencil to the fiducial marks on the panel.

The MPM Ultra Print 3000 was procured during Phase 2 and installed as the permanent dual-use screen printer on Flex 3. This machine met the requirements for printing on 20 mil pitch components, maintain process Cpks in excess of 1.33, and facilitates quick changeover.

Screen print evaluations where performed during Phase 2 to determine the best stencil configuration for the PNP and FEC boards and optimize the apertures to screen-print solder paste onto boards that incorporated various device technologies, including twenty (20) mil pitch "gull wing" leaded devices, fifty (50) mil "J" leaded devices and ball grid array devices. In addition, the screened solder paste deposit had to be optimized for the connector and cross over lead attach process. These evaluations resulted in use of a 6-mil stainless steel stencil with laser cut apertures laser cut for 25 mils and smaller and chemically etched for larger. Alpha WS 609-90-M13 solder paste was selected for PV because it is the facility's standard water soluble paste and it met all printing and process requirements during the earlier investigations. BGA pads were "overprinted" (BGA pad is 24 mils in diameter, solder aperture is 32 mils in diameter) to increase the solder volume. This avoided stepped stencils (multi-thickness stencils) and achieved Cp/Cpk values for fine pitch pads. For connector and crossover pads, split apertures were used to reduce the crowning of reflowed solder on these pads and avoid shorts. DV builds were made with these stencil parameters for the process.

Two types of problems were encountered during the DV builds of the PNP and FEC boards that were solved by additional modifications of stencil apertures for PV builds. The first problem noted was extensive solder balling on type 805 and 1206 chip resistors and capacitors. This was resolved by changing the rectangular apertures for these components to a "home plate" design, with the plate pointing inward. This

aperture reduced the amount of screened solder on the component pads by twenty (20) per cent and virtually eliminated solder balling.

The second problem experienced was high solder-joint defect rate (up to 10%) with components placed in topside thermally conductive adhesive (See OP #115). Analysis showed that these components could not "self-align" during solder reflow and leads were more elevated (a few mils) after reflow. This problem was resolved by increasing the amount of solder through increased aperture size. These adjustments were component type dependent and are summarized in the Table 5.4.2.2-1 below.

Table 5.4.2.2-1 Aperture Adjustment for Components with Adhesive

Board	Reference Designator	Comp Type	Pitch	Pad Size mils	Orig. Aperture	New Aperture	Incr. %
PNP A	U2,3,8,12,14	SOJ 36	50	25x60	45x60	45x80	33
PNP B	U4,5,9,10	SOJ 28	50	25x80	45x80	45x100	25
FEC A	U2,6,8,10, 14	SOJ36	50	25x60	45x60	45x80	33
FEC B	DC1,2	SOL 8	100	30x100	45x80	50x110	53
	G1	FP20	50	30x40	45x80	45x120	50
	U13	SSOP	20	14x60	12x58	13x58	8

The capability of the MPM 3000 screen printer to do two-dimensional checks on the screened solder pad area was also incorporated for PV builds. This is done 100 per cent on a representative set of screened paste areas and identifies screen problems real time. Solder defects were reduced significantly by these process steps (See Sec 5.4.4). As indicated in the Flow chart, solder dispense is a SPC controlled process and measurements are made and charted at the beginning of every build.

5.4.2.3 Topside Adhesive Dispense (Op # 115)

5.4.2.3.1 Top Side Adhesive Dispense

The IBP PNP and FEC printed wiring board assemblies contain several components each, which require a thermally conductive adhesive underneath to enhance the transfer of heat from component to the board. This requirement applied to SOJ36, SOJ28, SOIC FP and SSOP devices. Gaps to be filled with adhesive ranged from 0.005 in. to 0.050 in.

There was no in-house capability to dispense thermally conductive adhesive in the precise and accurate amounts required by the PNP and FEC printed wiring board assemblies. TRW Marshall had no existing requirements for any component adhesives

other than standard chip bond material (Loctite 3609) used to attach bottom-side chip capacitors and resistors on commercial products prior to wave solder.

During Phase 2, Loctite 5404, a silicone-based thermally conductive adhesive and a Cam/ALOT 2800 fully automatic, in-line adhesive dispenser were selected for this process step. Performing thermal adhesive dispense automatically and in-line provides several significant advantages. The amount and location of adhesive is precisely controlled. Placement of components on the adhesive by the automatic equipment is precise and repeatable assuring reliable thermal contact. It also avoids significant manual labor if it were done offline after solder reflow. These advantages justified the additional work required in adjusting solder stencil apertures (Section 5.4.2.2) and the somewhat higher solder joint defect repair required by these components (Section 5.4.4.3). Dispense process capability was established during Phase 2, and SPC data collected during builds, (See Sec 5.4.4).

5.4.2.3.2 Dispense Pattern Development for PV Builds

High levels of open solder joints for components with adhesive underneath during initial DV builds required process modifications to the dispense patterns of the adhesive, in addition to increasing the amount of screened solder paste as discussed above. Under-body gap between components and board surface for all components with thermal adhesive were analyzed and compared to dispense thickness. Thicknesses were reduced to still exceed max gap dimension to assure that contact is made with the adhesive during component placement. This was done empirically because the under-body gap typically has wide variation between components.

In most cases, linear slightly overlapping dispense patterns were used, covering about seventy (70) per cent of the underside of the components. This proved acceptable for all but the fifty (50) mil gap SOJ components. For these, a three-dot dispense pattern gave the largest reduction in solder joint defects. The final dispense parameters used for PV builds are shown in Table 5.4.2.3.2-1 below. Figure 5.4.2.3.2-1 shows actual dispense patterns on a board before component placement. Adhesive dispense is a SPC controlled process and data are taken and charted for every PV build. (See Sec 5.4.4)

Table 5.4.2.3.2-1 Adhesive Height and Dispense Patterns

Board	Ref. Designator	Component Type	Under-Body Gap (mils)	Dispense Height (mils)	Dispense Pattern
PNPA	U2,3,8,12,14	SOJ36	35/49	58±5	3 Dots
	U9,10,15	SOIC28	0/12	18±3	Lines
	AR1,2	SOL16	4/11	18±3	Lines
	U18,19	SS0P56	8/16	18±3	Lines
	E1	Custom2	5/9	13±2	Line
PNP B	U4,5,9,10	SOJ28	25/31	34±4	Lines
FEC A	U2,6,8,10,14	SOJ36	35/45	58±5	3 Dots
	U16,17	SSOP56	8/16	14±2	Lines
	E1	Custom2	5/9	14±2	Line
FEC B	AR1,3,4,5,8	SOIC8	4/10	14±2	Lines
	AR2,6,7	SOL16	4/11	14±2	Lines
	DC1,2	SOL8	5/9	14±2	Lines
	G1	FP20	5/9	14±2	Lines
	U8	SOP8	4/10	14±2	Lines

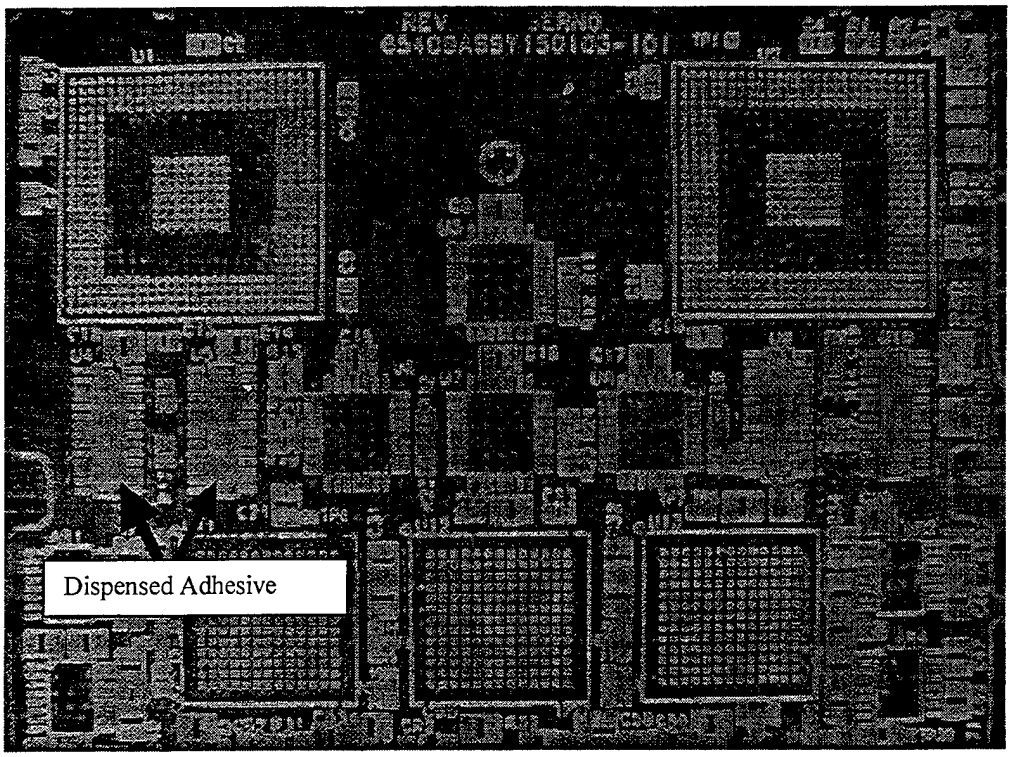


Figure 5.4.2.3.2-1 Thermal Adhesive Dispense Pattern

5.4.2.4 Component Placement Operations

Component placement for the four PNP and FEC boards is done on the in-line top-side onsertion portion of Flex-3. Three machines, the MV2, MPA, and GSM (see following operations) do all component placement with automatic feed. Components placed by each machine are based on machine capabilities. The MPA machine was specifically

added to Flex 3 to facilitate fast changeover between military and commercial products. Each machine is initially programmed by a machine set-up technician in preparation for DV builds, based on inputs from the product engineer, and using placement data from Gerber files from board layout data from ASD. Placement capability data were evaluated for all three machines for certain component types and are documented in Sec 5.4.4.

5.4.2.4.1 Component Placement Set-up

At the beginning of a build the factory machine controllers for the IBP-MPLC CIM system are activated. The bar code of a product panel to be run is scanned in at OP #90. This alerts each placement machine for the product type and loads the correct build files. Line operators set up each placement machine by scanning in component feeders to the correct feeder slots as required by the software program on the machine for this build. This feature is exclusive to the CIM system on Flex 3 and is currently only used for building PNP and FEC printed circuit assemblies. It mistake proofs improper material loading and hence placement on the board. When all material/feeders have been scanned in at each machine, the placement machine is ready for operation. Hard copy set-up sheets are available at each station for back-up use by operators.

5.4.2.4.2 MV 2 or Topside Surface Mount Onsertion (OP #120)

The Panasonic MV2 component placement machine is a twelve (12) position-head, five (5) nozzle per head turret-style machine. After pickup of a component, the turret head rotates clockwise. Component height, location on nozzle, and rotation is checked by the vision system before placement. Placement occurs with factory set force. If a component is rejected during pre-placement check, it skips placement and is ejected into a reject bin. Before the next pickup, a turret head transitions through nozzle select and nozzle origin ready. No changes were required to meet PNP and FEC board assembly requirements other than the feeder bank capacity was increased to meet the number of parts on the bill of material. The MV2 places about 60 to 80 % of the components on each board. The components are exclusively 805 and 1206 resistor and capacitor chips. Placement rate is about 5 components per second. No significant placement issues were experienced with the machine.

5.4.2.4.3 MPA or Top Side Surface Mount (OP #123)

The Universal MPA placement machine was added to Flex 3 in order to meet the 15-minute per station change over goal. The machine provides 57 additional feeders so that the added components can reside on the line or be set-up before machine changeover.

The machine was placed on line for PV builds in Phase 3; placement capability is shown in Sec 5.4.4. The MPA grips and centers components with three mechanical jaws. Improperly gripped or misaligned parts are placed in a reject bin. For PNP A, PNP B, and FEC A board assemblies the MPA places 7 to 13 percent of the components. For the FEC B assembly, the MPA places about 35 per cent of the components. Components placed are resistor chips, resistor networks, electrolytic caps, inductors and diodes. No specific placement difficulties were encountered with this machine during PV builds. Highest rejected components were diodes, which have a round cylindrical body with rectangular end caps.

5.4.2.4.4 GSM or Fine Pitch and BGA Placement (OP #125)

The PNP and FEC boards require the placement of various 25 mil and 20 mil pitch PLCCs, ICs and 50 mil ball grid array (BGA) devices. The GSM has the capability to pick and place these components.

While the GSM places from 6 to 20 percent of the total components on each of the boards, they are essentially all the active ones, totaling 20 to 30 components per board. Delivery is from reels on feeders and depending on the board, from 2 to 7 are fed from the Ramtf tray feeder. The 100, 50 and 25 mil pitch devices were well within GSM demonstrated placement capability. The capability to place 20 mil pitch and BGA devices was evaluated during Phase 2 of the project since it was not standard manufacturing practice in the plant.

After exiting from the GSM machine, the two-board panel halts in queue at an inspection station for visual examination by a line operator. This in-line inspection is performed by a trained operator, and for DV builds, is in accordance with ANSI/IPC-A-610 Rev B, class 3 visual requirements. The operator looks for component absence, presence, correct polarity, and proper on-location component placement. The objective at this station is for the operator to monitor the prior component placement operation to verify machines are working correctly. This inspection is performed at line throughput rate.

5.4.2.4.5 GSM 20 Mil Pitch Capability

The FEC B board is the only one with a 20-mil pitch component, a 56-leaded TSOP device. During DV and PV builds device placement met requirements. Visual inspection of solder joints noted some incidence of opens. This resulted in modifying the stencil aperture to increase the amount of solder paste by eight (8) per cent for PV builds. PV results met requirements.

5.4.2.4.6 Ball Grid Array Placement

The PNP and FEC boards were the first AEN Marshall product to use ball grid array (BGA) devices. The GSM machine on Flex 3 had the handling and vision recognition capability to place BGAs, and this was demonstrated and documented in Phase 2. Placement process Cpks met or exceeded the 1.33 requirement.

The biggest problem experienced with BGA placement on the GSM during both DV and some PV builds was a high frequency of rejection of some BGA types by the vision system. The eight BGA types used in the product were of different sizes, solder ball counts, array types and came from two different suppliers. Experience accumulated during DV and PV builds strongly pointed to illumination level of the solder ball array for pattern recognition as a critical parameter that had to be adjusted.

For example, the BGA components with perimeter arrays have an array of heat sinking solder balls in their center. These typically reflect more light and had to be excluded from the pattern in order to recognize the perimeter solder balls. Also the level of illumination had to be adjusted empirically from BGA lot to lot or for those from different suppliers to optimize vision system discrimination and reduce vision rejects.

In the interim between DV and PV builds, the software on the GSM was upgraded. This upgrade allowed the machine now to pre-orient (rotate) parts before the vision system alignment step and thereby eliminated errors associated with rotation after vision system check. Also it provided the set–up technician with the capability to "teach" components to the GSM rather than use only the CAD neutral file data. This was useful in trouble shooting and diagnosing vision reject and placement issues. Due to the high cost of BGA components, vision system rejects were returned to the loading trays and recycled.

5.4.2.5 Topside Reflow (OP #130)

The reflow temperature profile for the Alpha water soluble WS609-90-M13 flux and the Flex 3 Line Electrovert Atmos 2000 convection forced air reflow oven was developed prior to the initial DV builds. A five (5) position mole is sent through the oven to measure the oven profile before each build during DV and PV following established plant procedures. This profile is checked against the requirements previously established and documented in the set-up procedure. The reflow profile with specified parameters is shown in Figure5.4.2.5-1

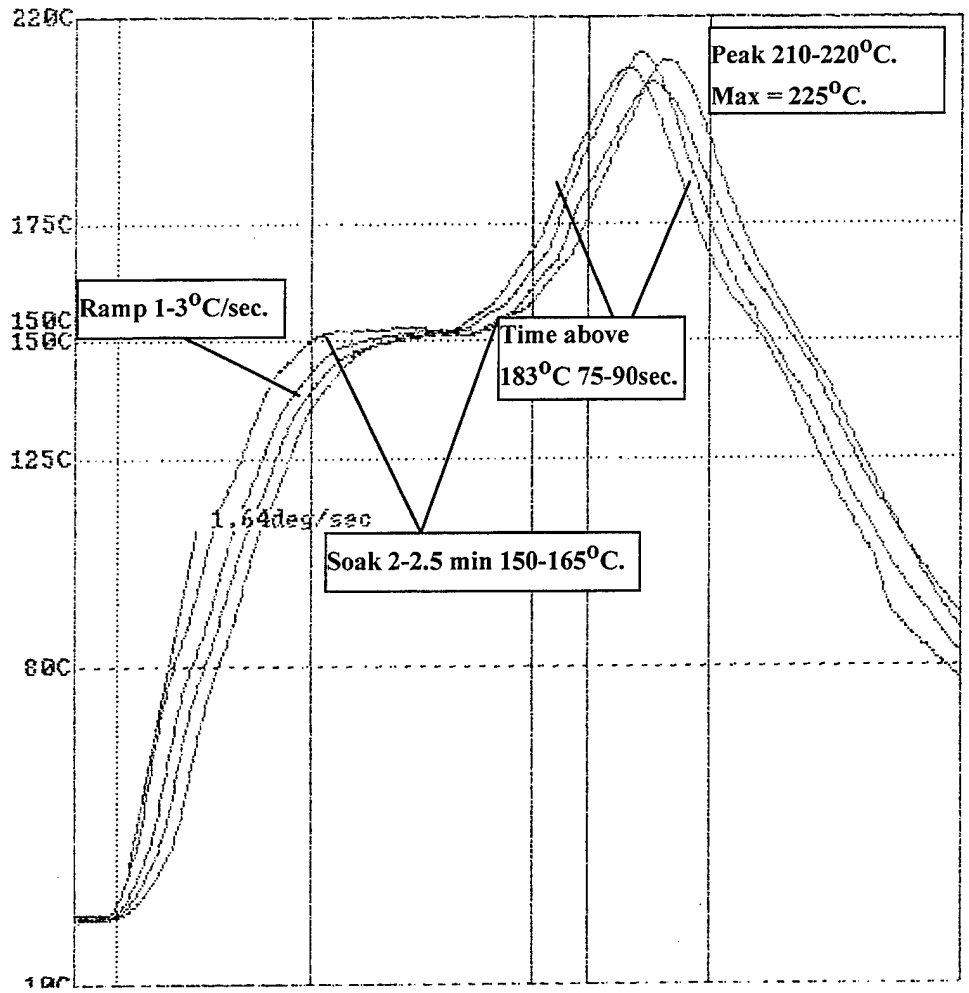


Figure 5.4.2.5-1 Electrovert Atmos 2000 Profile for WS609-90-M13 Solder Paste

5.4.2.6 Inspect/Touch up solder joints (OP #135, #136)

Upon exiting from the reflow oven, the two-board panel halts in queue at an inspection station for visual examination by a line operator. A trained operator performs this in-line inspection, and for PV builds it is in accordance with IPC-A-610B Class 3 specification. Defective solder joints or other defects identified, may be manually reworked by the inspector. Examples of such defects may be open solder joints, wrong parts, incorrect polarity, etc. These defects and resulting rework are also logged (by scanning in the board bar code label and manually entering the data on the reworked component) in the CIM system. This provides a database for defect tracking and process improvement.

5.4.2.7 *Flex 3 Changeover for Operations 110 Through 130 for Dual Use Production*

A requirement for the IBP-MPCL program is that line changeover for the Flex 3 operations 110 through to 130 inclusive will be less than 15 minutes for each operation. Through analysis of changeover times at each station at DV and PV builds, this requirement was met and typical changeover times by operation are as documented in Table 5.4.2.7-1 below.

Table 5.4.2.7-1 Flex 3 Line Changeover Times by Operation

Ops #	Equipment / Process	Changeover Minutes *	Comment
110	Solder Paste Printer	10	Change Stencil, Program, Add Paste
115	Topside Adhesive Dispense	2	Change from Pass-through
120	MV2 Component Placement	10	Remove 2, Add 2 Feeders
121	MPA Component Placement	2	Change from Pass Through
125	GSM Component Placement	14	Remove 7, Add 7 Feeders
136	Reflow Solder Oven	5	Re-stabilize profile
330	Cascade DI Clean	0	Use As Is

*Note: Changeover time based on switching from Model MAC14 assemblies.

5.4.2.8 *Aqueous Clean (OP #330)*

Existing Flex 3 line equipment is used to clean the PNP and FEC board assemblies after solder reflow. This operation removes the water-soluble flux by washing the boards with deionized water. The equipment used is a multi-wash, multi-rinse and dry in-line system. Each two-board panel is carried through the system in a wire mesh basket, component side up. The process steps and parameters are shown in Table 5.4.2.8-1. Panels or boards pass through this wash-dry cycle at four ft./ min.

Table 5.4.2.8-1 Aqueous Clean Parameters

Chamber	Temperature, ° F	Pressure, PSI
Wash 1	145 ± 10	20
ISO Airknife		20
Wash 2	145 ± 10	20
ISO Airknife		20
Rinse	145 ± 10	20
ISO Airknife		20
Final Rinse	145 ± 10	20
Airknife 1,2,3		20 each
Dryer 1 Oven	155 ± 10	
Dryer 2 Oven	155 ± 10	

To verify the effectiveness of the clean cycle and per the process control chart, one or more boards per DV or PV build were tested for cleanliness (ionic contamination) using the in-house ICOM 5000 test station. The test is performed with a solution of alcohol /water at 47 ° F at a rate of 40 ml per square inch of panel area plus allowance for components (an additional fifty percent of area). The pass criteria is less than 10.7 μg NaCl equivalent per square inch. During PV one build of boards failed this test. This was traced to incoming board cleanliness. Tests were run which established chlorine ion contamination due to inadequate cleaning by the board supplier. Assembled boards were submitted to an additional cleaning cycle to pass. Subsequent panels were checked during incoming for cleanliness before use on Flex 3. One group of panels required additional cleaning before assembly use.

5.4.2.9 X-Ray Sampling (OP # 376)

In AEN Marshall's present surface mount technology, processes are run with sufficient process control (high Cpk) such that visual inspection is only done as a monitoring step. In the plant's current surface mount technology, virtually all solder joints are readily visible. Since the reflowed solder ball connections in ball grid array devices are under the component and not readily visible, high Cpk processes (solder paste deposition, component placement and reflow) were developed as described. However, in case of process problems, x-rays can be used to detect some ball grid array solder defects. The plant's low level x-ray inspection system is adequate for solder ball shorts, gross defects and misalignments. Figure 5.4.2.9.1-1 shows a BGA x-ray including a pair of shorted

balls. After board assembly only a sample of boards were examined to monitor the reflow process. If the boundary scan in-circuit testing (See Sec. 5.4.3.1) indicated BGA shorts, x-ray was used to confirm these before performing any rework.

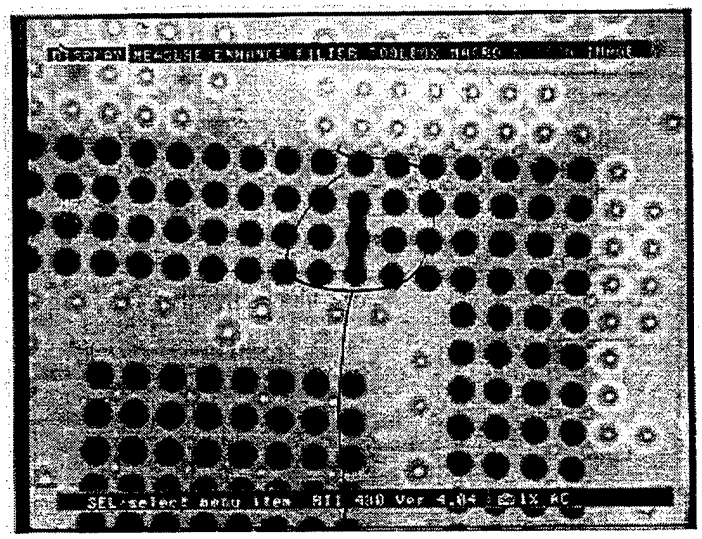


Figure 5.4.2.9-1 X-ray of BGA Connections with Shorted Solder Balls

5.4.2.10 PCB Singulation (OP #420)

The PNP and FEC boards are assembled on Flex 3 with two boards per panel. A router is used to remove the breakaway, or excess board material of the panel (the singulation process) by cutting through the webbing that connects the PWB to the breakaway. A Cencorps TR1000 router was installed during Phase 2. This router is used in stand-alone operation. Two mistake proof panel fixtures have been designed, one to accept only PNPA/FECA panels, and the other only PNPB/FECB panels. The correct panels are loaded component side down into the mistake proofed product specific fixture as shown in Figure 5.4.2.10-1, which is seated in the router. The routing operation is performed from the top while debris is removed with vacuum suction. Using the wrong software program could easily destroy a PNP or FEC board, therefore, mistake proofing was added during Phase 3. Each fixture is bar coded. Before the routing operation begins, the fixture barcode is scanned and verified against the loaded routing program. Routing proceeds only if fixture and program match up. To verify the set-up a "dummy panel" is placed on the fixture, and routed.

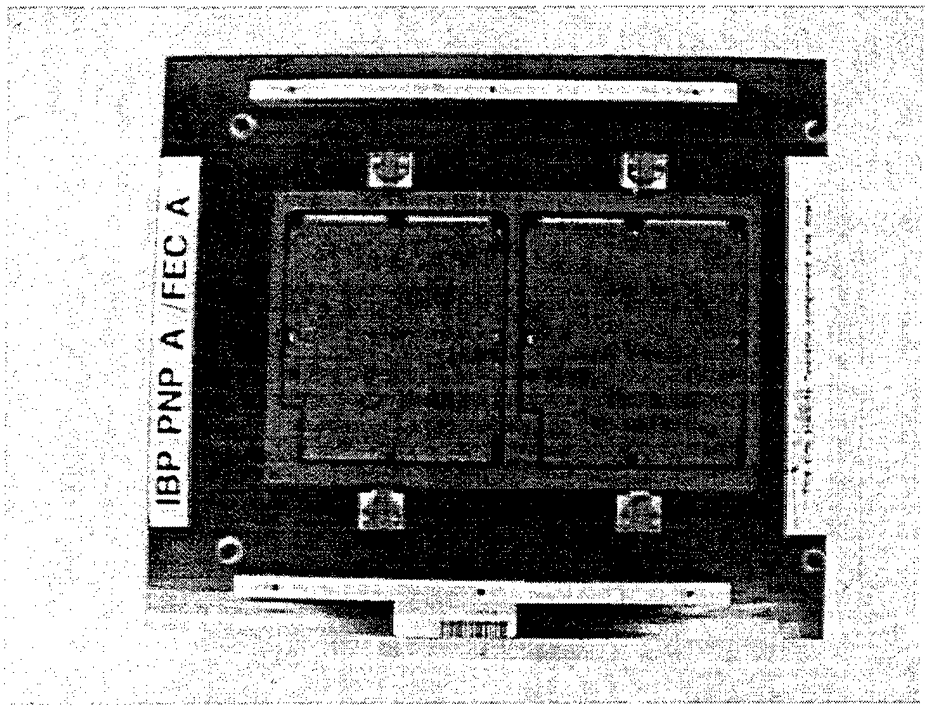


Figure 5.4.2.10-1 Panel in Routing Fixture

5.4.2.11 In-Circuit Test/ Boundary Scan (OP #430)

In-circuit testing (ICT) is a standard process step in all commercial board assembly manufacturing. ICT provides a number of very important advantages. Defects can be detected at the front end of the manufacturing line and specifically identified. Functional final test yields are increased. Failure analysis and repair costs are minimized. Process quality levels are effectively monitored and summarized. Due to the potential for design changes at DV affecting test fixturing, ICT was implemented with PV level builds.

ICT requires bed-of-nails fixturing and test software development. Due to test engineering resource limitations, the test software development and test fixturing were subcontracted under the supervision of a AEN, Marshall test engineer. (Test software for commercial products is subcontracted as well for similar reasons.) The proofing of test fixturing and software are facilitated by known good boards.

To obtain known good functioning boards two sets of PNP A/B and FEC A/B boards were assembled to thermal cores. Instead of using curable adhesive, the complete assembly was done with thermal grease (allowing later disassembly). The two sets of PNP and FEC modules were sent to ASD for functional testing. Upon verification that these modules performed functionally, they were returned to the plant and disassembled

and cleaned to remove the thermal grease. The subcontractor, to debug the test software and fixtures at his facility, then used these "known good" boards.

Debugged test software and fixturing was installed and proofed at Marshall under the supervision of a test engineer on the Flex 3 GenRad 2284 test system. See Figure 5.4.2.11-1 for a board in a test fixture. The board is precisely positioned with alignment pins. An array of probes (bed-of nails) contacts the test points on the bottom side of the board while the board is held down with vacuum and pressure probes from the top.

PV level board assemblies were tested (as defined by the test software) for opens, shorts, passive, and active component values and tolerances, as well as active component functionality. The TRW AEN plant has extensive experience with this type of testing. High pin count BGA ASICS, which are boundary scan compliant, are checked using boundary scan testing; this was a new test methodology to the facility.

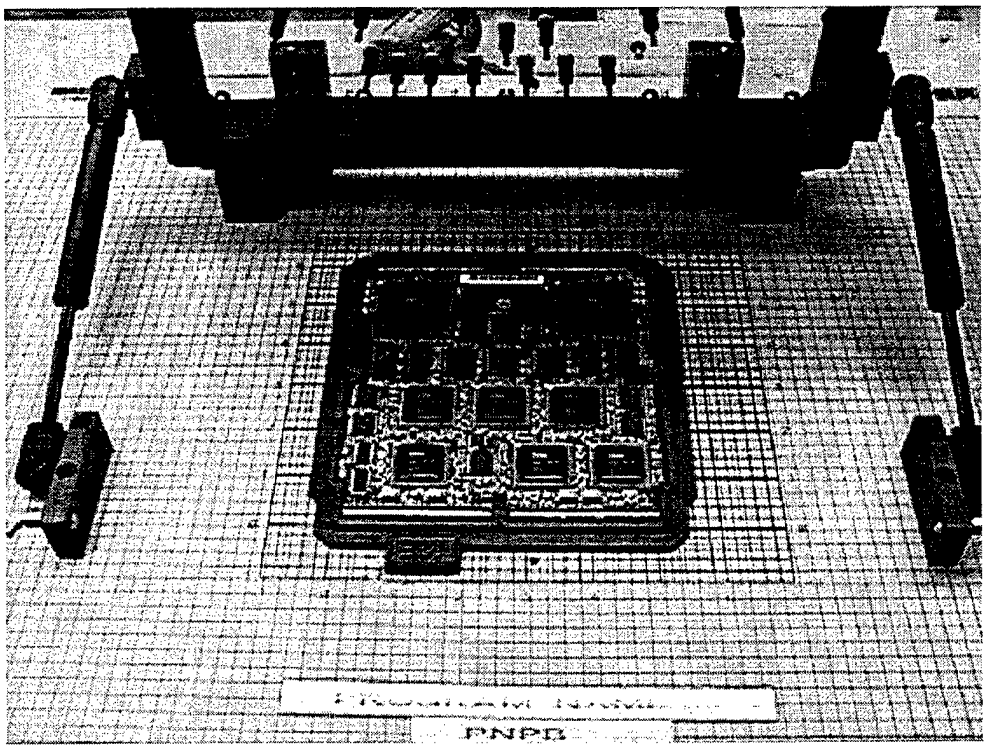


Figure 5.4.2.11-1 Board Assembly in ICT Fixture on GenRad.

For boards failing ICT, a failure report is printed, which identifies defective components for rework. Upon rework completion, the board is re-tested.

Actual test times were quite short for such complex digital circuits. Times varied between eleven (11) and thirteen (13) seconds. Some probe fixturing contact problems were experienced, primarily traceable to the use of 0.035 in. diameter test pads. Probes sometimes had to be "tweaked" in order to make contact. A more robust design of 0.05 in. diameter test pads would eliminate this problem.

5.4.2.12 Rework (OPs #136, 957)

Due to the high bill of material cost, defective PNP and FEC PV boards identified in process visual inspections or at ICT were reworked. Defective components other than BGAs can be readily removed and replaced by existing processes and equipment using operators certified in soldering and workmanship criteria. With rework, a total of 257 of 268 boards passes ICT (96%).

Defective BGA required special equipment and process development for removal and replacement. An SRT Summit 2000 rework station was set up in early Phase 3. This equipment has the capability to selectively heat a BGA for removal and replacement. For each BGA type and location on the PNPA, PNPB, FECA and FECB boards, a separate heating profile was developed and programmed using station software. Heat is applied to the board by a heater from the bottom raising its temperature to 140°C. Additional heat is applied by hot air from the top by a custom nozzle specific to each BGA size. To get the nozzle around the BGA, some chip components on the perimeter of the BGA have to be removed. After removal of a BGA, the solder pads have to be dressed to remove excess solder. The BGA area is then fluxed, and a new BGA replaced by a pickup arm. Alignment of the new BGA to its pads is done by viewing images of the solder balls and pads simultaneously using a split-image mirror system. This critical step is done manually. Final placement of the BGA and the reflow cycle is done under program control. After BGA replacement, removed peripheral chip components are replaced manually before re-testing the circuit board.

5.4.3 Module Assembly Processing

Module processing is a separate offline operation dedicated to PNP and FEC module assembly. An L-shaped work cell was set up with dedicated workspace for each of the assembly operations (See Figure5.4.1.1-4). Work cell controller stations were strategically placed at certain work areas to facilitate prior-step scanning per the flow chart. Completed modules are packed for shipping in this area.

5.4.3.1 Core Bonding

To assemble the PNP or FEC modules, the two single sided boards (PNP A and PNP B or FEC A and FEC B) are bonded to a thermal core. Improvements were made in the processes from the DV to the PV builds.

5.4.3.1.1 Liquid Adhesive Application (OP #442)

The bond layer must meet at least 90% surface area coverage between board and core, and produce an adhesive bondline thickness of 0.005 in. to 0.008 in. Loctite 5404 silicone adhesive was selected during process development in Phase 2. During DV

builds the adhesive was screened to the back of the boards using a 0.010 in. thick stainless steel stencil. The stencil pattern consisted of apertures 0.093 x 0.093 in. separated by 0.012 in. grid and covered the entire board area. A deHaart semi-automatic benchtop screen printer was used. This pattern gives coverage of 78 percent between board and a glass plate surface (simulating a metal core). There was a higher than desirable voiding in the pattern due to the 0.012 in. grid.

To reduce the voiding a change was made, enlarging the apertures to 0.303 x 0.303 in. with a 0.012 grid spacing, and reducing the stencil thickness to 0.007 in. This provided 92.5 % coverage with significantly reduced voiding. To reduce adhesive bleed-out around the edges, the stencil pattern was reduced by 0.1 in. at the perimeter. Figure 5.4.3.1.1-1 shows the new stencil pattern. A "sample" is screened to verify adhesive thickness (0.007 in +/- 0.002 inches) and to check the set-up of each stencil in the deHaart screen printer. For efficiency, all the A boards are screen printed with adhesive, followed by a stencil change and the B boards. To promote the adhesion of the Loctite 5404 to the cores, the cores are prepped by wiping each surface with Nusil Primer CF1-135 and curing.

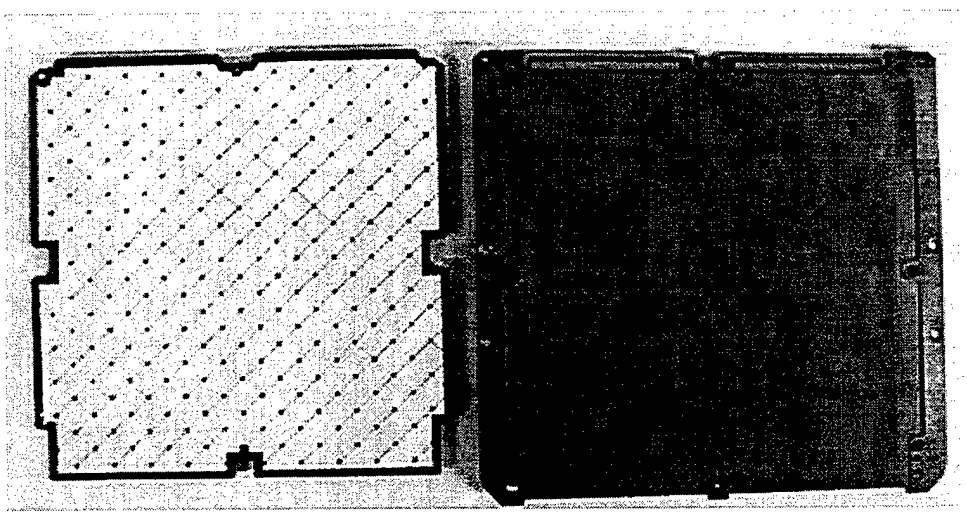


Figure 5.4.3.1.1-1 Board with Thermal Adhesive Applied and Thermal Core

5.4.3.1.2 Mechanical PCB Assembly (OP #447)

Attachment of the A and B boards to their respective sides of the prepped core is a manual operation. Alignment between the boards is maintained by inserting three (3) pins through alignment holes in both boards and the core. This pin alignment maintains the ± 0.003 mil registration between the connector and cross over pads on the A and B boards. It also assures that the boards are bonded to the correct side of the thermal cores. The pinned board-core assemblies are placed in a vacuum bag for adhesive cure.

5.4.3.1.3 Liquid Adhesive Cure (OP #448)

A vacuum bag process is used to apply pressure to the boards and core during cure. Up to six board-core assemblies can be placed in the vacuum bag during the adhesive bond cure. (See Figure 5.4.3.1.3-1). The vacuum bag with assemblies sits on a supporting tray and is placed into an oven pre-heated to 130 ° C. A vacuum hose is attached and the bag is evacuated to a pressure level of 9 ± 1 psi. Vacuum pressure is adjusted with a bypass valve. This pressure was empirically found to give minimal bleed out of adhesive and an optimal bond line thickness of about 0.006 mils after cure. The cure cycle is one hour. After cure, the assemblies are removed from the bag and allowed to cool to room temperature. Any small amount of adhesive bleed-out around the board edges is manually removed.

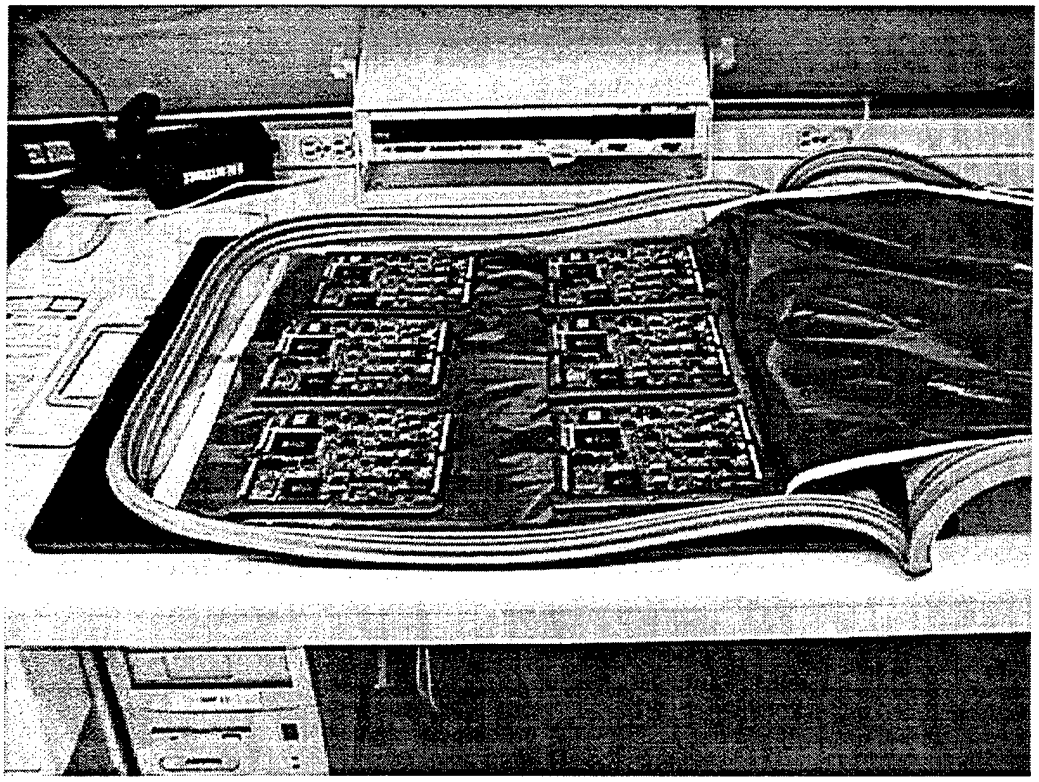


Figure 5.4.3.1.3-1 Board-core Assemblies in Vacuum Bag

5.4.3.2 Mechanical Assembly and Hot Bar Process

The processes to attach high pin count, 25 mil pitch connectors and flexible crossovers (to electrically interconnect the A and B boards) are described here. These processes are performed manually by a certified solder operator, assisted by mechanical fixturing and optical magnification. Soldering the backplane connector, requires the alignment of up to 90 leads, 8 mils wide, to pads 18 mils by 150 mils at one time. For the FEC

module, three co-axial RF cables and a ground lug are added. All processes are performed at dedicated stations set up in the final assembly area.

5.4.3.2.1 Mechanical Assembly (OP #561)

At the beginning of Phase 3, the fixture to align and facilitate the attachment of the Bendix two-section, 360 lead, connector to the core-bonded assembly was finalized (See Figure 5.4.3.2.1-1). This fixture holds the connector, while the assembly is put on a slide. The assembly is locked in place on the slide and the slide is moved to insert the end of the boards with the connector pads between the 180 sets of connector leads. As received, the gap between two opposing tie-bar connected connector leads is 0.090 in. The thickness of the core-bonded assembly is 0.150 in. As the assembly was inserted between the connector leads, the spreading of these 8 mil thick leads from 0.090" to 0.150" increased tension and could cause them to slip off the reflowed solder on the 18 mil pads. The operator then had to re-align these leads individually increasing process time. A "lead-spreader" block was added to the fixture. The tie-bar connected connector leads are first inserted over the 0.250 in. block, which has the effect of opening the leads from 0.090 in to about 0.135in. This wider opening allowed the subassembly to slide between the leads with minimal lateral deflection. With the subassembly between the slightly deflected connector leads the operator uses the adjustment knobs on each side to center the 180 leads over the pads on the board with the help of optical magnification. This is made possible since the leads are tie-bar connected and maintain relative position to each other. The core-bonded assembly was pinned during the adhesive cure to within 0.003 in, so the upper and lower connector pins are aligned simultaneously. The connector is secured with three screws maintaining the lead to pad alignment during the hot-bar solder reflow process.

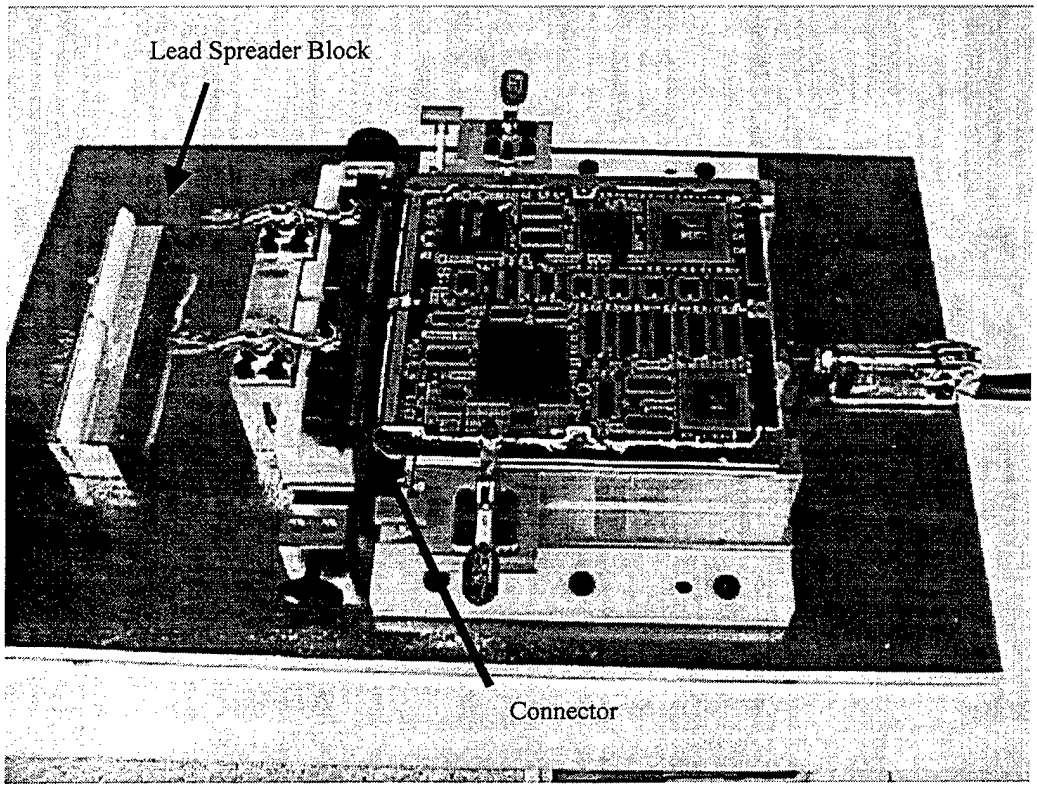


Figure 5.4.3.2.1-1 Connector to Core-board Assembly Alignment Fixture

5.4.3.2.2 Selective Solder / Mechanical Assembly (OP #564)

To solder the connector leads to the board, the board-core assembly is transferred to a fixture in the ToddCo hot-bar station and locked in place as per Figure 5.4.3.2.2-1. A video monitor with magnification is available at this station to check the lead-to-pad alignment. The operator must also set-up and align the hot-bar to the connector leads. Alpha water soluble flux paste (WS619) is applied manually using a syringe. (Solder is not required, since it was added and reflowed in the required amount during board assembly on Flex 3). Solder reflow is performed with the hotbar tool using the programmed heating profile and pressure shown if Figure 5.4.3.2.2-1. Upon completion of the reflow cycle, the operator manually grips and "breaks off" each tie-bar from the leads.

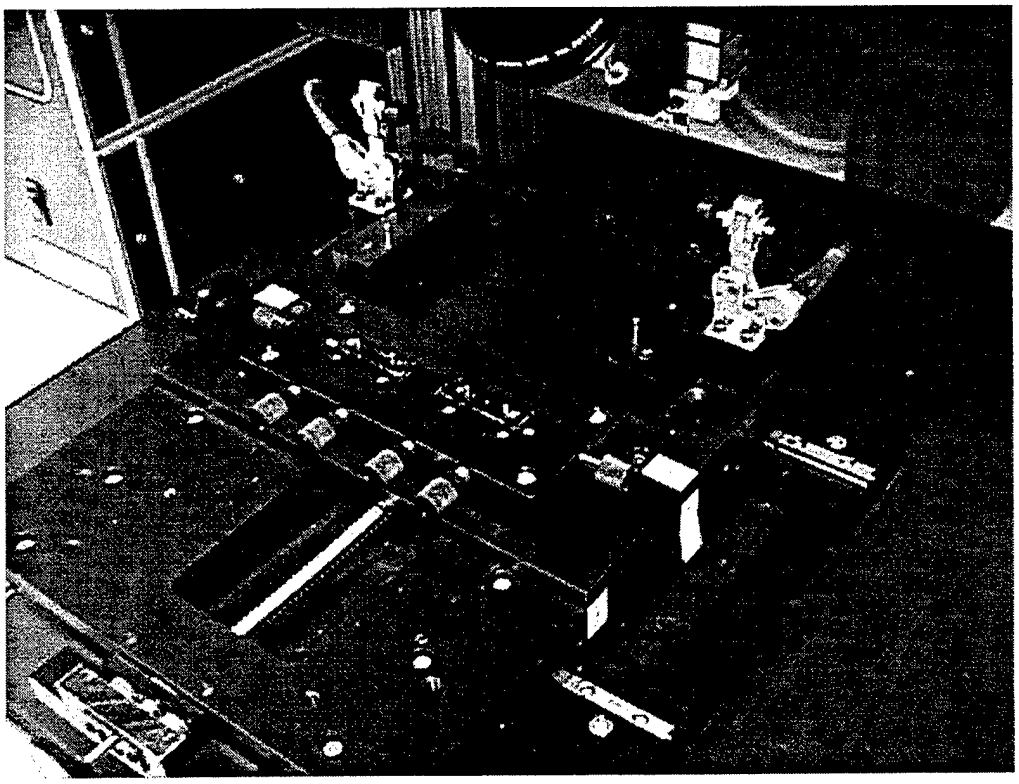


Figure 5.4.3.2.2-1 ToddCo Hot-bar Fixturing

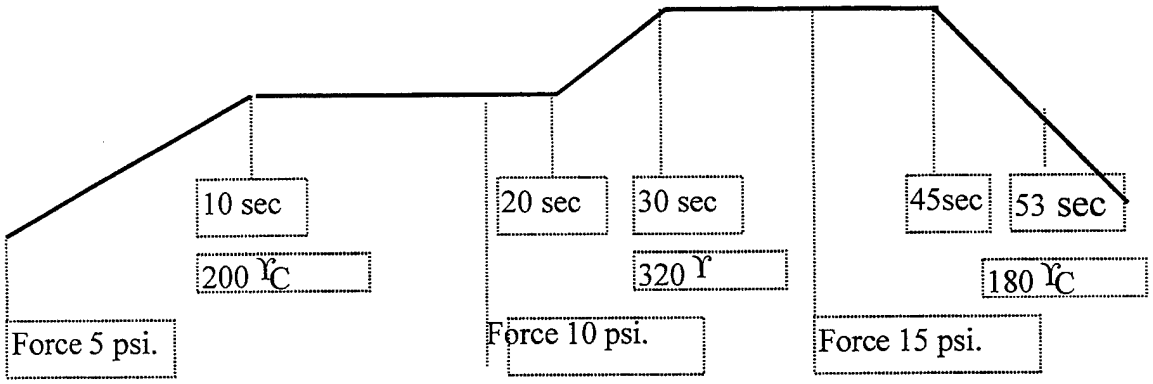


Figure 5.4.3.2.2-2 Hot-bar Temperature and Pressure Profile for Connector Leads

The four crossovers are aligned and soldered to the board pads using the same fixture on the ToddCo station but with a different hot-bar tool and solder profile. The fixture can relocate the board-core assembly to bring the crossovers under the hot-bar tool. The crossover has thirty-eight (38) 10 mil leads, which are aligned to 18 mil x 125 mil pads. There are tie-bars at each end of the crossover leads. Alignment of lead to pad is again critical and facilitated by the tie-bars. Figure 5.4.3.2.2-3 shows the fixturing detail that was added to facilitate the holding and alignment of the crossover during solder reflow.

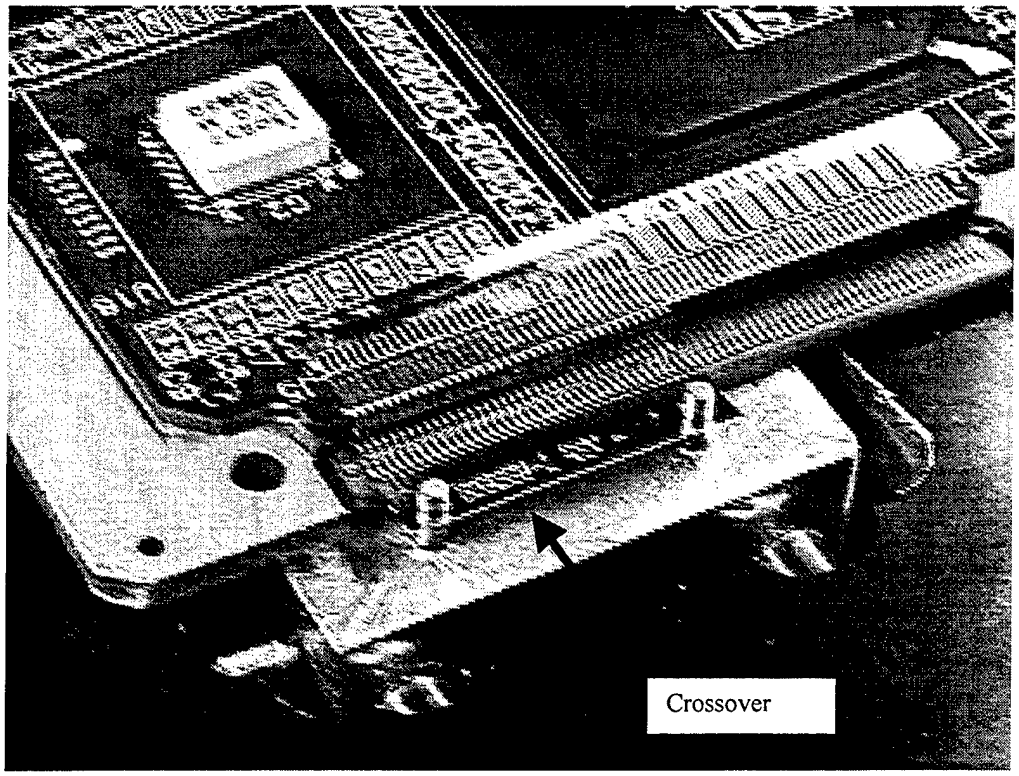


Figure 5.4.3.2.2-3 Fixture Detail for Crossover Soldering

The crossover is placed over the positioning pins. Alignment is made viewing a video camera image and using the micro-screw adjustment. Alpha water soluble flux paste (WS619) is manually applied by using a syringe and reflow is performed by the hot-bar under computer controlled profile. The upper leads are reflowed first. The fixture can reposition the board-core assembly to four locations to get all four crossovers under the fixed hot-bar head. The hot-bar height must be set-up for upper and lower boards separately. Visual aids on the fixture aid the operator in these set-ups. After completing the solder-reflow for the upper and lower leads, the operator manually removes the tie bars at each end.

5.4.3.2.3 Inspect (Touch-up Bendix Connector/ Flexible Crossover (OP #575)

After the connector and crossover soldering on the ToddCo station, a certified operator visually inspects the solder joints under a microscope. If required the operator will do solder touch-up under a microscope using a standard soldering iron and water-soluble flux and solder.

5.4.3.2.4 Coaxial Cable and Ground Lug Attachment (OP # 578, #582)

Both these operations are only applicable to the FEC module. They are manual and performed by a trained operator in the final assembly area. During DV builds, cables were cut and stripped by the operator. For the PV builds, the three co-axial cables were

cut to precise length to fit the routing. Shielding and insulation were stripped by TRW ASD. Each cable was labeled for mistake proofing during installation. Visual aids in the process instructions aid the operator in the installation of the cable and ground lug.

5.4.3.2.5 Aqueous Clean and Module Bake (OP #587 and #589)

Modules processed through connector, crossover and cable attach need to be cleaned to remove the water-soluble flux. This cleaning process is identical to Operation #330, and outlined in Section 5.4.2.8. The Bendix connector has extensive recesses that can trap water that may not be removed by the air-knife segments and dry segments in the in-line cleaner. Blow off and bake step for 1hr at 130° C ± 5 ° is performed to remove all water from all recesses of the module.

5.4.3.3 Final Module Assembly

5.4.3.3.1 Final Mechanical Assembly and Serialize Module (OP #730)

Completion of module manufacture requires some additional mechanical hand assembly. During Phase 2, final assembly was completely manual. In Phase 3, a mistake-proof fixture was added to facilitate final assembly. The fixture, shown in Figure 5.4.3.3.1, holds the wedgelocks in correct orientation for attachment to the module. Removable threadlocker for the wedgelock screws was added for the PV builds. A Mountz manually held torque screwdriver is used to set screws to the specified torque requirements. The ejectors and polarized keys in the connector are still manually installed for PV modules.

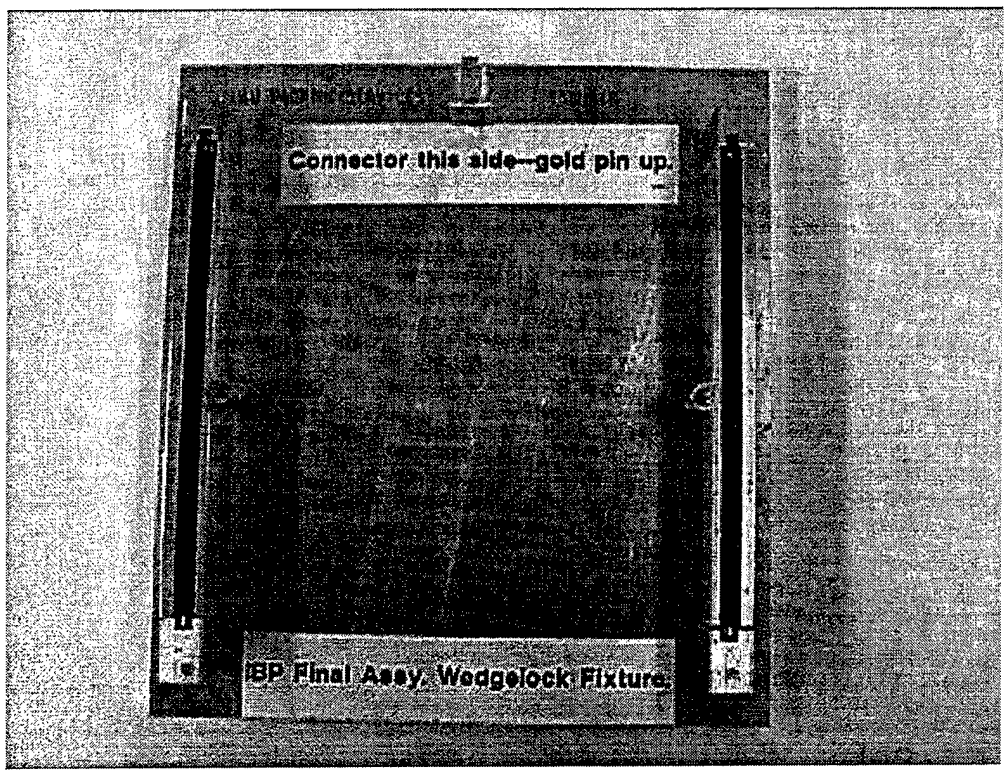


Figure 5.4.3.3.1 Final Assembly Fixture for PNP and FEC Modules

Upon completion of the final mechanical assembly, the bar codes on the two printed circuit boards are scanned at a work cell controller (WCC) tying the two serial numbers together in the CIM data base. The B board is scanned, bottom cover is attached, and the module placed in the final assembly fixture. The A board is then scanned, after which a bar code printer prints two module-level bar code serial numbers with revision levels. One label is applied to a designated area on the "A" side cover, the other on the outside of the shipping container.

5.4.3.3.2 Pack and Ship Modules (OP #730 and #990)

Packaging utilizes an anti-static molded container that houses the completed module assembly. (See Figure 5.4.3.3.2-1) This container is then inserted into a corrugated partitioned shipping box surrounded with a shock gap on the sides. Partitions were designed with mistake proofing in mind. The container only fits in the partition one way. See Figure 5.4.3.3.2-2 packaging details. This packaging protects the module for shipments between AEN, Marshall, and ASD, San Diego.

This packaging method was expected to fully protect the modules in transit. In the process of transporting the modules, approximately 10% were damaged. The module damage was consistent to the ejector-mounted corners of the thermal core. Levels of module damaged varied from hairline cracks of the thermal core to complete fractures. One module had both ejector corners fractured.

The cause of the damage was not determined. Some shipping containers showed evidence of violent handling (gashed corrugation, dented corners) and some of the anti static molded containers showed evidence of damage. These did not correlate to all cases of damaged modules. Improper packing of the module into the molded anti static container was thoroughly reviewed and discounted. No method could be found to induce the loads necessary to crack the cores. Improper or flawed core material could not be evaluated or discounted.

Conformal anti-static shipping sleeves were acquired to replace the molded tote. Small quantities of modules were transported with these sleeves without mishap.

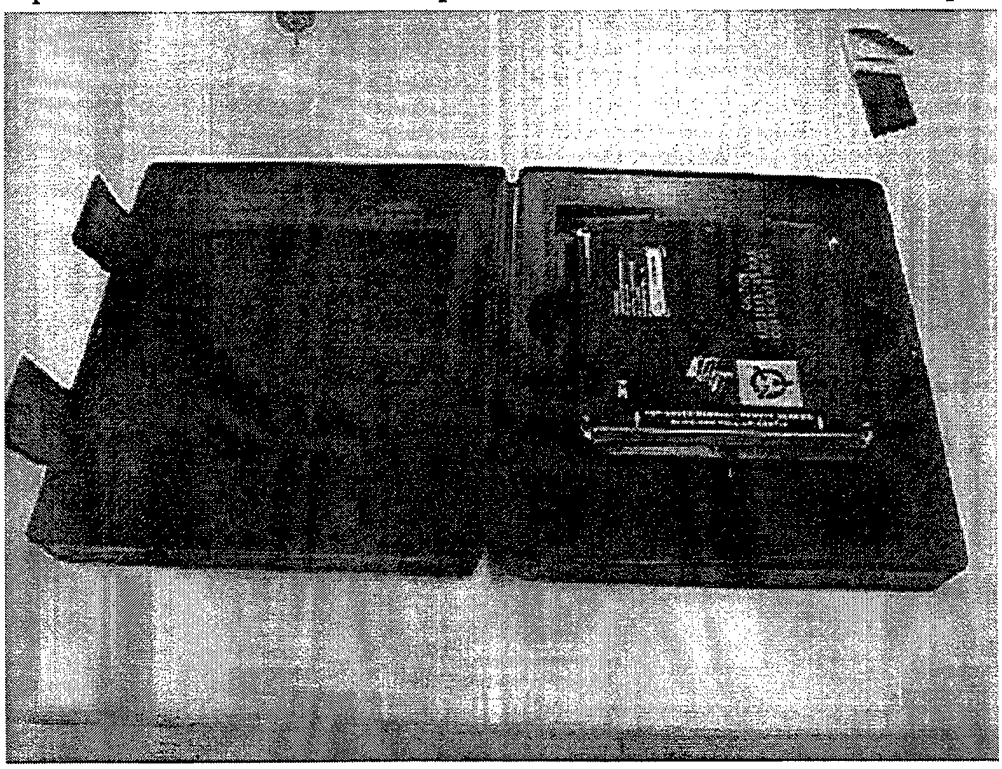


Figure 5.4.3.3.2-1 Anti-static Module Shipping Container

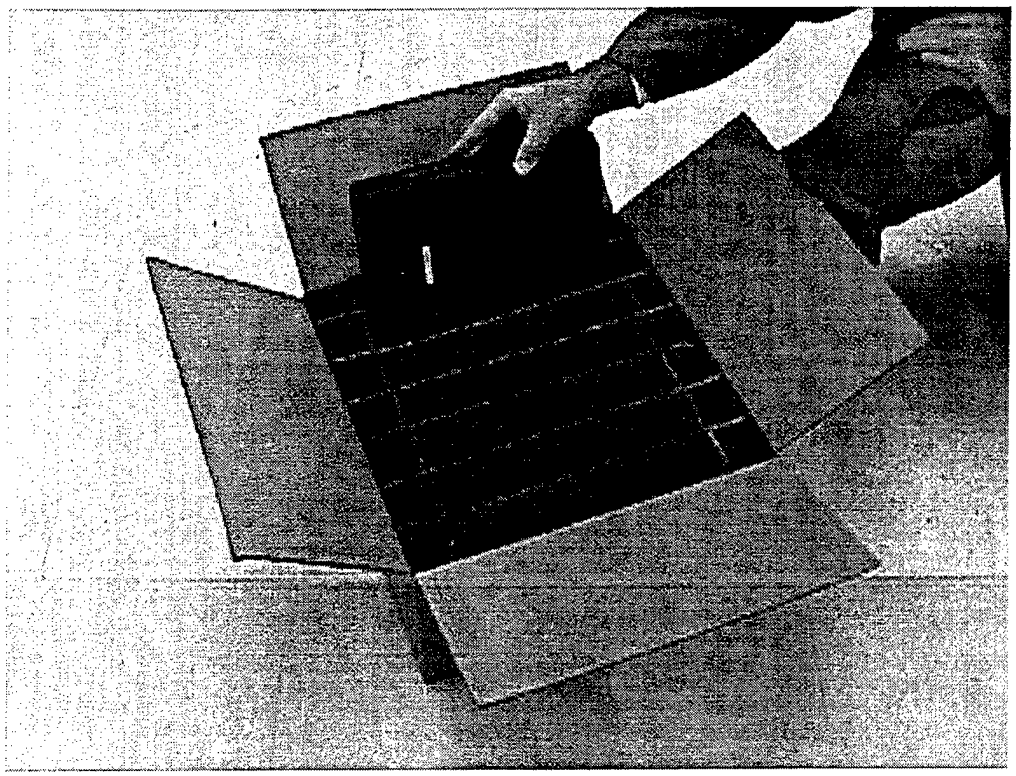


Figure 5.4.3.3.2-2 Shipping Box for Modules

5.4.3.4 ATP and ESS Testing (OP #952, #953, #981, #982, #983)

Module acceptance testing and environmental stress screening were performed on each module prior to delivery. These tests were performed at TRW-ASD prior to conformal coating at AEN. These tests are described in the Design Validation section of this document (Section 6).

5.4.3.5 Conformal Coating and Underfill

Commercial automotive circuit boards at AEN Marshall are coated to provide a moisture barrier. In-line spray or dipping systems are used to apply the material to the circuit boards. During Phase 2, epoxies, acrylics and silicone materials were reviewed. The standard Marshall material is an acrylic material (HumiSeal 1B31). However, for environmental reasons, studies were underway by Marshall plant process engineering to change to a silicone based standard material. A number of leading potential silicone replacements for the standard acrylic material had been identified (HumiSeal 1C55 and Dow Corning DC1-2577 Low VOC) and were evaluated on boards as part of DOE #2 study. Spray coating will not provide total undercoating for the BGAs, therefore, an underfill process was developed for these components. Thermal-only curing silicone (HumiSeal 1C55) was selected. DC1-2577 material was selected as the conformal coat.

5.4.3.5.1 Underfill of BGAs and Cure (OP #591 and #592)

HumiSeal 1C55 material is used for BGA underfill. The underfill process consists of dispensing material manually from a 10 cc syringe, along one side of a BGA, and letting capillary action wick the material underneath. Application from one side only eliminates trapped air bubbles. Increasing board temperature can accelerate the underfill wicking action. Accordingly, the boards are pre-heated and maintained at a temperature of 85 ± 5 ° C using the heater stage in the SRT BGA Rework station. Underfill continues until the material forms a meniscus around all sides of the BGA. After underfilling all BGAs on one side of a module board, the 1C55 is cured in an oven at 125 ± 5 ° C. The process is repeated for the BGAs on the other side.

5.4.3.5.2 Conformal Coat Spray (OP #596)

The DC 1-2577 Low VOC coating material is scheduled to be the main conformal coat material for the plant, and is applied by spraying with in-line automated equipment. A production coater was set-up and programmed to spray DC1-2577 material on DV boards and the process demonstrated. Change over involves swapping lines, pressure tanks and valves used with the standard acrylic material with a duplicate set for the DC1-2577 material to avoid contamination. This was very time consuming and a heavy production schedule limited access to this equipment.

The in-line spray process was replaced with a manual spray process using dedicated pressure tank and spray valve similar to what is on line. Prior to coating, the sections of the module that are to remain free of coating are masked. A "boot" is slipped over the Bendix connector, but the rail areas and ejectors are covered with removable tape that can withstand the bake temperature. For PNP and FEC module coating, the DC 1-2577 material is mixed at the ratio of four (4) parts material and one (1) part thinner. Tank and valve pressure was optimized for the process and material. The operator controls the process visually by making sure all areas are coated. DC 1-2577 material contains UV luminescent dye that is used to verify a continuous coating.

5.4.3.5.3 Conformal Coat Cure (OP #597)

Moisture activated cure begins almost immediately at room temperature, but the process is accelerated by a 30 minute oven bake at 70 ± 5 ° C. The DC1-2577 material is compatible with the 1C55 material under the BGA components. Due to the low viscosity of the coating material the topside must be fully cured before the part can be turned over for coating the other side. A coating thickness of three mils minimum is adequate for moisture protection, and this is readily achieved with this process.

5.4.4 Process Capability

5.4.4.1 Initial Capability Evaluations

During Phase 2, processes requiring initial capability evaluation were identified and included solder screen print, connector reflow, component placement and adhesive dispense. The target Cpk requirement was to equal or exceed 1.33. The results for these initial process Cpks are shown in Table 5.4.4-1

Table 5.4.4-1 Initial Critical Process Capabilities

Process	Actual Cpk
Solder Screen Print:	
50 Mil	2.10
BGA	1.89
25 Mil	1.74
20 Mil	1.65
Connector, Reflowed	1.69
Crossover, Reflowed	1.40
Component Placement:	
MV2	1.75
MPA	1.90
GSM	1.33
Adhesive Dispense:	
Length	1.36
Width	3.20
Height	1.46
Core Bond Line Thickness (Vac. Bag)	2.08

5.4.4.2 SPC During PV Runs

During the PV builds a number of processes were monitored statistically as per control plan. Measurements were taken after each set-up on the first article to be processed. The data was plotted on X-bar/R chart. Upon completion of the PV builds, the data was analyzed to determine the parameters for statistical control, and to evaluate process capability. Results are shown in Table 5.4.4.2-1. Actual X-bar came very close to the initial trial specifications. Capabilities for the actual process were calculated using X-bar and the initial tolerance specification. The control plan will be adjusted to the actual x-bar data.

Table 5.4.4.2-1 Actual Run Cpks for Critical Process per Control Plan

OP #	Process	Characteristic	Initial Specification Mils	Actual Process Prameters Mils	Cpk
110	Screen Solder Paste	Thickness	8 ± 2	7.7 ± 0.46	1.45
115	Topside Adhesive	Thickness	58 ± 5	58.1±0.93	1.79
			36 ± 4	35.4±0.70	1.90
			18 ± 3 in	17.4±0.54	1.85
			14 ± 2 in	13.7±0.47	1.40
442	Liquid Adhesive Application	Thickness	7 ± 2 in	6.5±0.45	1.48

5.4.4.3 Visual Inspection Results

The component placement and solder reflow process per control plan is monitored visually by trained operators using the ANSI/ IPC 610-A, Class 3 standard. Defects found were logged in the CIM system. A reject rate in parts per million (PPM) can be calculated by dividing total rejects by total number of solder joints.

The biggest solder joint defect was open joints or insufficient fillets associated with components with thermal adhesive underfill. Initially during DV, solder-joints defects for these components were as high as 100,000 PPM. By increasing the amount of solder paste and adjusting thermal adhesive height, the overall reject rate for adhesive underfilled components was reduced to 4950 PPM. The defect level for components without thermal adhesive underfill was 320 PPM. Of this quantity about 94 PPM is due to components being off-location, and about 62 PPM is due to solder shorts on J1 pads. The combined defect level for all components is 610 PPM of which half is due to components with thermal adhesive underfill. Reduction of this defect level could be achieved by using a thermal adhesive with a lower temperature coefficient of expansion, further pad redesign to increase the amount of solder, or possibly using an alternative solder paste.

5.4.4.4 Quality Model Predictions and PV Results

The quality model outlined in section 5.4.1.2.3 predicts the following defect levels for the two modules as shown in Table 5.4.4.4-1:

Table 5.4.4.4-1 Quality Model Predicted Defect Levels in PPM

	PNP	FEC
Defect Level, A Board	75,000	65,300
Defect Level, B Board	77,600	60,800
Defect Level Assembly	42,600	62,200
Defect Total	196,000	183,300
Defects Eliminated Through Verificaion	177,700	163,900
Defect Level to Customer	25,300	24,400

The defects in the A and B boards of each module results from the defect levels in the components (as shipped from the supplier) and placement/solder reflow process defects in the assembly process. Defect reduction through verification is accomplished by reworking defects found by visual inspection and in-circuit testing. From Table 5.4.2.11-1 the first pass rejection yield for the PNP A and PNP B boards is 270,000 PPM and 260,000 PPM. The Quality Model prediction is too low by a factor of three to four. The most significant reason for the difference was that the model assumed a 30 to 40 PPM process level defect level for chip components, 70 to 80 PPM for leaded components and 200 to 240 PPM for BGA components. PV results indicate a process defect level of 320 PPM for components without thermal adhesive underfill and nearly 5000 PPM for components with thermal underfill. The model did not correctly predict the higher defect level from to the introduction of the thermal underfill process. It also used somewhat lower numbers for the components without underfill. A higher level of in-process defects was experienced and visual and in-circuit test screens are required to detect these defects to reduce the level shipped. See section 6 for module ATP/ESS metrics.

5.4.5 Module Level BGA Rework

5.4.5.1 Process Characterization

Once the circuit board assemblies have been bonded to the thermal core, selective rework becomes more difficult, due to the heat sinking that occurs from the core. Most parts can be removed and replaced using standard rework methods with the addition of some preheating.

The BGA packages are a special problem for rework. The BGA packages are designed to transfer heat from the die into the heat sinking thermal core through the solder joints. However, these solder joints are not accessible to a soldering iron. Typically, localized

hot gas is used to reflow the BGA joints simultaneously. Rework systems focus hot gas on the part to be reworked, while shielded solder joints of surrounding parts.

5.4.5.2 Equipment

5.4.5.2.1 Rework Station

An Air-Vac DRS26 rework system is used for surface mount rework in the San Diego facility. The system has computerized control of the temperature and flow rate of heated nitrogen gas directed to the module surface through localized focusing nozzles sized to the outline of the part being reworked. The system also controls an air plenum for generalized preheat of the entire board surface and post-reflow cool down.

5.4.5.2.2 Modifications

The system, as marketed, was unable to provide enough heat to reflow BGA solder joints on thermal cores without damaging the BGA package. Two 500-watt core heaters with closed-loop temperature controllers were added to preheat the module.

Increasing the temperature of the thermal core allows reduction of the temperature of the focused nozzle heat while maintaining reflow temperatures at the solder joints. The reduction of the focused nozzle heat reduced the amount of warping in the BGA packages.

Ramping the temperature of the module quickly under closed loop control is important to remain within solder paste reflow processing windows. The module is able to quickly stabilize at a preheat temperature without exceeding reflow temperatures.

Thermal blankets with heat shields were also added to cover the entire module. They reduce temperature variations over the module surface by diminishing ambient air and by redirecting the focusing nozzle exhaust.

5.4.5.3 Process Development

Due to the thermal mass, the reflow temperature cycles are longer than those recommended by solder paste manufacturers. Solder pastes and gel fluxes were tested for solder balling and wetting per IPC-TM-650, with the additional condition of subjecting the pastes to the extended reflow temperature cycles necessary for cored module rework. The samples with solder that wet the copper the best without slumping or solder-balling excessively were selected.

Tests were also done to identify the ideal deposition of solder paste on the pads in order to have enough paste to act as a thermal bridge but not so much as to cause solder bridging and shorts. Experiments compared dispensing and printing of solder pastes

and gel fluxes. A four-mil stencil with .025 inch solder paste apertures was selected to give the right and consistent volume over the hundreds of pad locations for each BGA.

Another process developed was preparation of the BGA pads prior to part replacement. Excess solder left on the pad from the old BGA part must be removed from the pad, leaving a flat, solderable surface. Wicking off the solder with copper braid left pads with reduced solderability. Solder vacuum pumps with hollow soldering iron tips damaged the surrounding solder mask. The rework system manufacturer supplied a non-contact vacuum system that left flat, solderable pads without distressing the solder mask.

5.4.5.4 Results

Attempts were made to rework BGAs on the DV modules while the module level rework process and functional tests were being developed. As a result, only 66 percent of the 9 FEC DV modules reworked and 44 percent of the 9 PNP DV modules were successfully recovered to a working condition. Typically, larger packages were less successful than smaller, and glob-top packages more difficult than overmolded. The largest glob-top package, the BGA352, had only two successful replacements out of fifteen attempts. Table 5.4.5.4- 1 shows the BGA Rework performed by part type.

Table 5.4.5.4-1 DV Module BGA Rework by Part Type

Part	Package	Attempts	Success	Rate
C31	BGA169	5	3	60%
DMAD	BGA169	6	2	33%
MTC	BGA225	5	3	60%
NBP	BGA256	5	2	40%
CBIU	BGA313	5	2	40%
MAME	BGA313	7	4	57%
DSP	BGA352	7	1	14%
RTP	BGA352	8	1	13%
TOTAL		48	18	38%

Typically, if the module was not repaired with the first BGA rework attempt, it was not likely to be ever recovered to working condition. There was only one case of a module with multiple rework being restored to working condition. This is partially due to deteriorating pad solderability with every rework and partially due to the uncertainties of the functional test diagnostics.

Rework was not attempted on non-functioning PV modules due to poor process yield.

6.0 DESIGN VALIDATION

Verification of the functionality and operational capability of the IBP-MPCL product was a major effort. Testing and analysis was performed to insure product integrity and ability to perform in all required environments. Verification testing performed on the hardware falls into two primary categories.

Manufacturing verification tests are primarily electrical tests that are performed at each level of assembly (component, circuit card, and module) to drive out problems at the earliest level of assembly possible and to insure product integrity. Much of this electrical testing is performed on a 100% basis and is required for acceptance of the hardware to the next level of assembly or delivery.

Design verification tests are those tests required to validate the design. These tests are electrical and mechanical tests run on a sample of the designs and are intended to validate the design as a whole. These tests are conducted over severe use environments where it is not practical to do 100% testing.

6.1 Manufacturing Verification Tests

6.1.1 Component Testing

The majority of the microcircuits used for these designs were standard (off-the-shelf) and required no additional testing to validate functionality. For these devices, the manufacturer typically guarantees performance over the specifications called out in the published datasheet. This is substantiated either by functional testing of the delivered product or by initial technology characterization testing. When testing is performed, it is typically done on a sample basis for mature product designs and for only a limited set of key functional parameters.

For this design there were some microcircuit devices that required additional testing beyond what the original part manufacturer performed. These fell into two general categories; custom microcircuits that were repackaged to accommodate the commercial, low-profile, surface mount design (i.e. PBGAs) and standard, off-the-shelf microcircuits that had a commercial-rated operating temperature range (0°C to +70°C).

For both of these categories, validation of product qualification and reliability testing was necessary prior to additional functional verification testing. In the case of the custom microcircuits, the original die technologies were evaluated for acceptable failure rates and the PBGA package technology qualification data was reviewed. For the standard, off-the-shelf devices, the supplier qualification and reliability data was evaluated for acceptability in the use environment.

6.1.1.1 ASIC Testing

ASIC die manufactured by Motorola for the military program were packaged into ball grid array packages by IBM for the IBP-MPCL program. For the military program, Motorola made the ASIC die, packaged the parts and tested them. Test vectors were in the UTIC (universal tester interface) file format. These files could not be translated into a recognizable format for the HP tester at IBM without the purchase of a software conversion tool. Another path was to use the QuickSim data developed for ASIC simulation. These serial vectors for the Identification tests, Built in Self Test (internal BIST), and external interconnect (input/output driver test) could be translated to IBM's tester format. Therefore, the QuickSim data was translated and used. Understanding the peculiarities of the QuickSim format and determining when to clock the data were the biggest obstacles to overcome. For the DSP input/output test, it was best to break the test into a driver (output) test and a receiver test. IBM's tester halted when both of these sections were run together. Once the test vectors were translated, the parts were tested at -40°C, room ambient and +85°C. These test parameters along with the DC electrical test parameters are specified in each of the ASIC SCD (Source Control Document).

Due to yield loss during the packaging phase at IBM, the quantity of bare die became a concern. A second source, AMI, was added to supplement the Motorola die. AMI is a licensed third party for Motorola H4C. AMI started with transfer of the databases for the NBP, DSP, and the RTP ASICs. After translation of the database, new die were fabricated. The Mustang and UTIC test vectors that were created for Motorola, were required to completely test the die. The Mustang vectors had little documentation, and became a roadblock in validating the die. The testers used by both Motorola and AMI were thought to be compatible, but Motorola's vector format was unreadable with the software used by AMI. Cadence was contracted, as a third party, to perform the translation from Mustang to UTIC format for AMI. This translation was performed only for the DSP ASIC to minimize risk while AMI continued to create translation files manually. Due to re-direction of another TRW program, additional Motorola die became available to IBP-MPCL, and the AMI die became spares. To save cost, the AMI program was stopped, and both the tested die and untested die became spares for the IBP-MPCL program. The spare AMI DSP ASICs were tested and sorted, but the RTPs and the NBPs were not tested.

The DMAD ASIC is a dual monolithic analog to digital converter with offset and gain control and built-in JTAG. The DMAD experienced yield problems when tested after packaging. The original test procedure on this 169 BGA part resembled a design validation rather than a production validation run. The procedure specified 181 tests desired to be performed in less than three minutes. Besides continuity and basic DC

tests, the linearity and slope of the converter was tested at nine gain and offset settings. The internal digital pipeline was tested along with the JTAG 1149.1 interface. Finally, the signal to noise ratio and spurious response was tested. Noise glitches were seen on the tester at the test house, but this could not be reproduced at TRW ASD during module level testing with the DMAD, or at die level probing of the DMAD wafers at TRW Space Park. Different noise reduction techniques were tried from passive filtering to software filtering. The original part specification was modified to account for test set noise. The parts were also difficult to test at cold, due to frost and moisture problems on the test fixture. The result was a lower than expected DMAD yield, and a large effort was put into test and retest of the packages.

6.1.1.2 C31 Testing

The C31 (TMS320C31) processor was repackaged into a 169 PBGA by IBM. An Elf board software development emulator along with a Texas Instruments XDS500 development card was used in a standard IBM 386 PC as a test set. TI provided the test routines for the C31 processor with their XDS500 board. Minor modifications were made to the test software by TRW that allowed the packaged C31 to be tested. Modifications to the Elf card involved removal of the on board C31 (which was in a quad flat pack) and replacement with a PBGA adapter socket. This adapter was mounted with an angle bracket to the Elf development board. Testing of each C31 is performed by inserting the device, powering the PC, and running the Confidence Check Code. The resultant yield from this testing was 82%.

6.1.1.3 Other Parts

As a result of the part selection process for the two module designs, there were four other microcircuits that required additional screening and testing to validate their functional performance.

These four devices were designated as commercial temperature range (0°C to 70°C) components. For each of these devices no alternates were available that performed the same desired function over industrial temperature range and still met the other necessary design criteria (package dimensions, surface-mountable, durability, reliability and cost).

6.1.1.3.1 Motorola 4 Meg SRAM (MCM6246WJ20)

The Motorola 4 Megabit, 20 nsec SRAM selected for the FEC and PNP modules met the necessary design requirements of 25 nsec access time with less that .150 package height. In addition, these devices had extensive reliability testing by the manufacturer.

This included temperature cycling, moisture testing and high temperature operating life testing. However, this device was not rated by the manufacturer to perform at temperatures below 0°C or above 70°C. In order to obtain functional data over a wider temperature range, the inventory of 516 SRAMs were submitted to a third party test house and subjected to functional testing at -40°C and +85°C. Testing consisted of static, dynamic and timing tests at 20 nsec. The final results indicated that 515 of the 516 devices passed all functional test parameters at -40°C and at +85°C. The one remaining device was physically damaged during the testing process and thus not testable. Durability and production testing has yielded no failures due to a faulty SRAM.

6.1.1.3.2 IDT PLL Clock Driver (IDT74FCT88915TT70PY)

The original PLL clock driver designated for this design was a 55 MHz version. This device was specified to meet a 500-psec output skew over the commercial temperature range (0°C to 70°C). The application required output skew of ±1000psec over the wider operating temperature range, in particular, at low temperature. Per the application engineer's recommendation, the PLL device with the next higher operating frequency of 70 MHz was chosen.

Test engineering conducted a series of low temperature tests on the 70 Mhz device and found that the device did not deviate beyond the specified value of 500psec. Durability life and production testing to date has yielded no anomalies due to this part.

6.1.1.3.3 IDT FIFO (IDT72241L-35JC)

For the PV design, there was a switch from the 35 nsec part to the 25 nsec version of the same device type, since the faster part is offered in an industrial temperature version (IDT72241-25JI). Circuit analysis was performed to determine that the faster speed and slight increase in current draw were acceptable. Durability life testing to date on the PV modules has shown acceptable results without anomalies.

6.1.1.3.4 Cypress PROM (CY7C277-xxJC)

The original module design for the PNP required the use of a 40 nsec, 32K x 8 registered PROM. Cypress Semiconductor was the only manufacturer that offered this device. Cypress offered this device in the commercial temperature range, with availability for the industrial range based on demand. The program demand was not sufficient for the manufacturer to justify and configure to test the device over the wider temperature range. A faster 30 nsec commercial temperature version was selected as the 40 nsec part was discontinued. Pre-PV testing was used to validate the performance of this device at low and high temperatures (i.e. -40°C to +85°C). The results on the

durability modules and the production validation modules indicate no low temperature operational failures.

6.1.2 ICT

In-circuit testing on the GenRad is part of AEN's standard procedure. For PV modules, in-circuit testing is incorporated to identify manufacturing defects and to identify any fundamental part problems. The GenRad tester uses a bed-of-nails fixture that can probe each net on the backside of the printed circuit board to verify opens and shorts, identify correct part placement, and perform limited functionality prior to the board to core assembly process.

The complexity of the IBP-MPCL modules required new methods of test to be developed and added to the GenRad tester. One of these was boundary scan using the JTAG bus. BSDL (boundary scan) models, which have been developed for the ASICs at ASD were modified for use on the GenRad tester. Off-the-shelf devices containing boundary scan were ordered for test development. Off-the-shelf component .bsdl models were available from the vendor. AEN built fixtures to perform trial tests on these parts. The manufacturing section of this report has additional information on the in-circuit test process development.

ICT software and hardware development require known good PWB assemblies. Two modules of each (PNP and RF/FEC) were built on greased cores and functionally tested at ASD. The connectors were then removed and the modules were separated into boards and shipped to AEN. AEN worked with these "golden boards" to develop tests and tolerances for their in-circuit tests. GenRad developed the test fixtures and the test software for these boards. GenRad Engineers validated the software at AEN on the GenRad tester.

For PV testing, AEN developed test software to program the Cypress CY277 PROMs. AEN's GenRad tester was able to supply the necessary 12.5 volts for programming, but due to the inability to tri-state the outputs of the driving DMAD ASIC, this task could not be performed at ICT. Bus contention problems may have damaged the DMAD ASIC. Programming these PROMs was performed on a manually operated Data I/O programmer. The MTC EEPROM was also planned to be programmed by the GenRad. This would have eliminated the need of using the CATS Test Set programmer at ASD. Because of a bus contention problem, the MTC ASIC could not be tri-stated resulting in the programming of the EEPROMs as part of module test at ASD.

Several escapes of the ICT were discovered when failures occurred at module level testing. One of the JTAG tests that was discussed, but missed as part of in-circuit test, was the JTAG BIST (built-in self test). This test is needed to perform validation of the

internal gates of the ASICs. Without this, ASIC internal failures would go undetected until module checkout, where rework is exceedingly difficult. This occurred on 4.8% (4 of 83) of PNP modules that were built. Another escape of in-circuit test was that the DMAD ASIC did not recieve functional testing. An analog waveform could have been injected, and the resultant digital output could have been monitored while using different gain and offset conditions. The DMADs had a low yield in packaged part testing that ranged from 35 to 65%. Since the yield was so low, ICT should have included functional testing of the DMADs. Module testing uncovered DMAD failures on only 2.4% (2 of 83) of the modules.

Table 6.1.2-1 summarizes the ICT test results and shows the percent of boards passing the first time.

Table 6.1.2-1 ICT Test Yield PNP and FEC boards.

			Board Assmbly					
Pass/Fail	PNPA		PNPB		FECA		FECB	
Pass	No.	%	No.	%	No.	%	No.	%
P, 1st	63	73%	63	73%	32	67%	26	54%
P, 2nd	11	13%	7	8%	8	17%	12	25%
P, 3rd.	6	7%	4	5%	1	2%	6	13%
P, 4& >	3	3%	9	10%	3	6%	3	6%
P, S/T	83	97%	83	97%	44	92%	47	98%
Fail	3	3%	3	3%	4	8%	1	2%
Total	86		86		48		48	

Most board assemblies passing on the second ICT test pass had minor defects such as opens or shorts. These were readily reworked. Boards requiring three or more ICT-rework cycles had failures related to active components, such as ASIC opens or shorts. This requires replacement of the ASIC, a more complicated procedure. In a number of boards, the failures related to ASICS required extensive testing at ASD to identify the correct defective component. In summary, ICT detected no systematic problems with any specific component; defects were essentially random.

Finally, the FEC B software required some modifications to eliminate a problem with testing the MAME ASIC. This is the reason for the lower first pass yield for the FEC B board compared to the others. The PNP B software needed some modifications to eliminate relay malfunction on the tester. These problems suggest that a more comprehensive review of test fixturing and software with the contract supplier and the design team is desirable.

6.1.3 Acceptance Testing (ATP)

The test philosophy for the IBP modules includes a systematic progression of automated tests followed by manual verification of the failures. After ICT, the boards were visually inspected for opens and shorts on the parts, connectors and crossovers. The first test employed at TRW ASD was the opens/shorts test. This test measured pin to pin resistance at the connector, pin to ground and power for each signal. These values were compared to acceptable high and low values and a Pass or Fail is assigned. If shorts cannot be located by visual means, X-ray or thermal scans are used. Figure 6.1.3-1 shows a picture of a module in the ATP test stand.

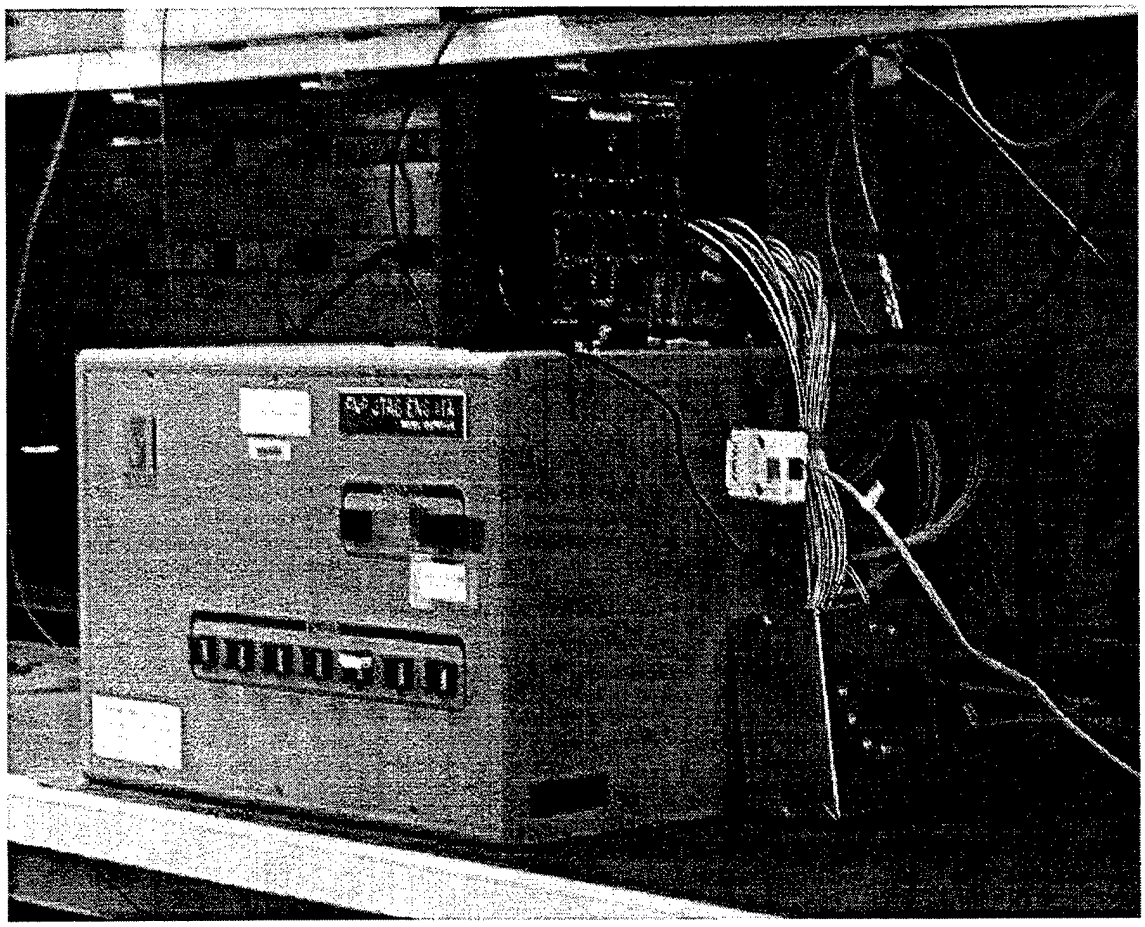


Figure 6.1.3-1 ATP Test Stand

6.1.4 Environmental Stress Screening (ESS)

After completion of the Acceptance tests, the module undergoes ESS (environmental stress screening) which includes 3 axes vibration and ten temperature cycles. Approximate test time (assuming no failures) using the Design Verification Test Station at ASD are as follows: ATP requires 2 hours; vibration 4 hours; and temperature testing

16 hours. Following ESS, a post-ESS ATP was performed, and the modules are shipped to AEN for conformal coating. The modules are shipped back to ASD for final ATP, then ready for delivery to the customer. Figure 6.1.4-1 and 6.1.4-2 show a picture of the ESS thermal and ESS vibration test set-up, respectively.

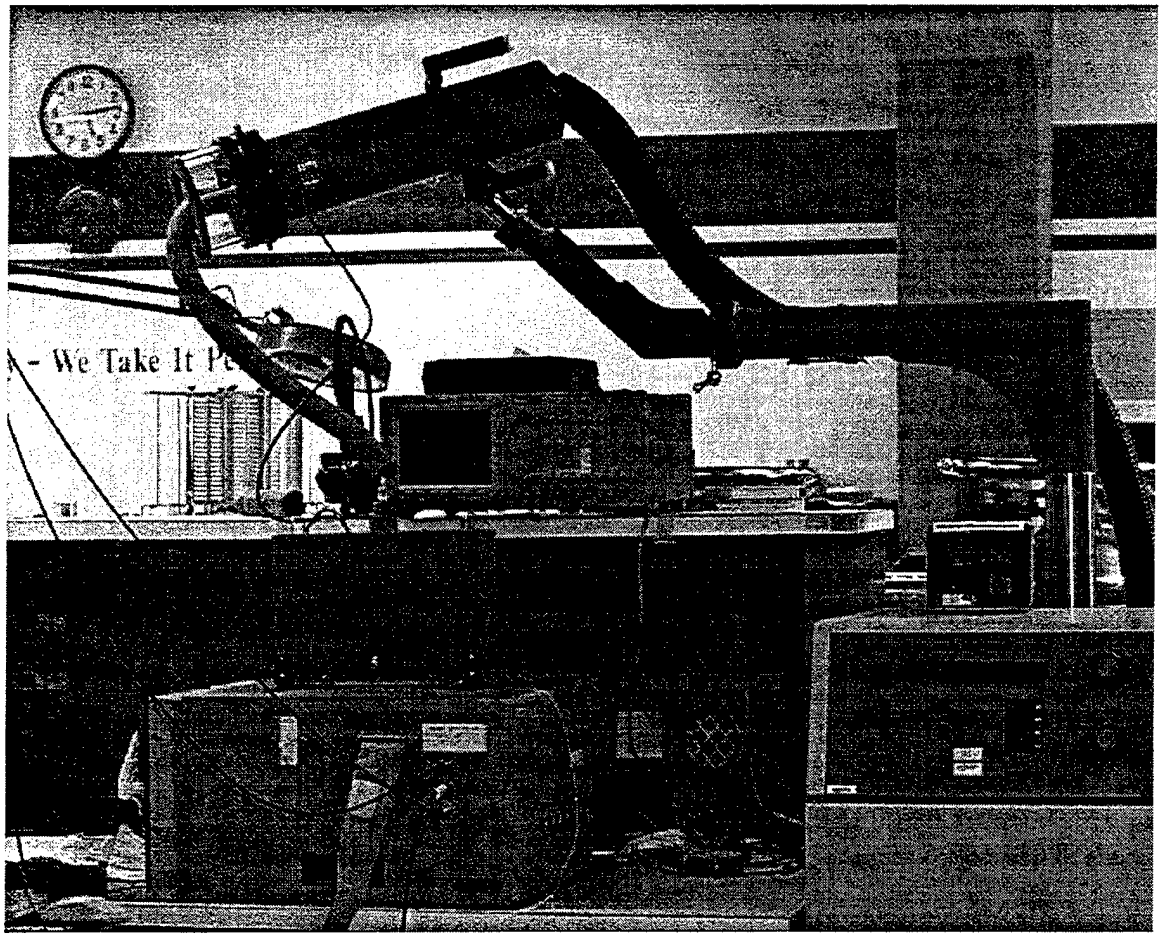


Figure 6.1.4-1 ESS Thermal Test Set-up

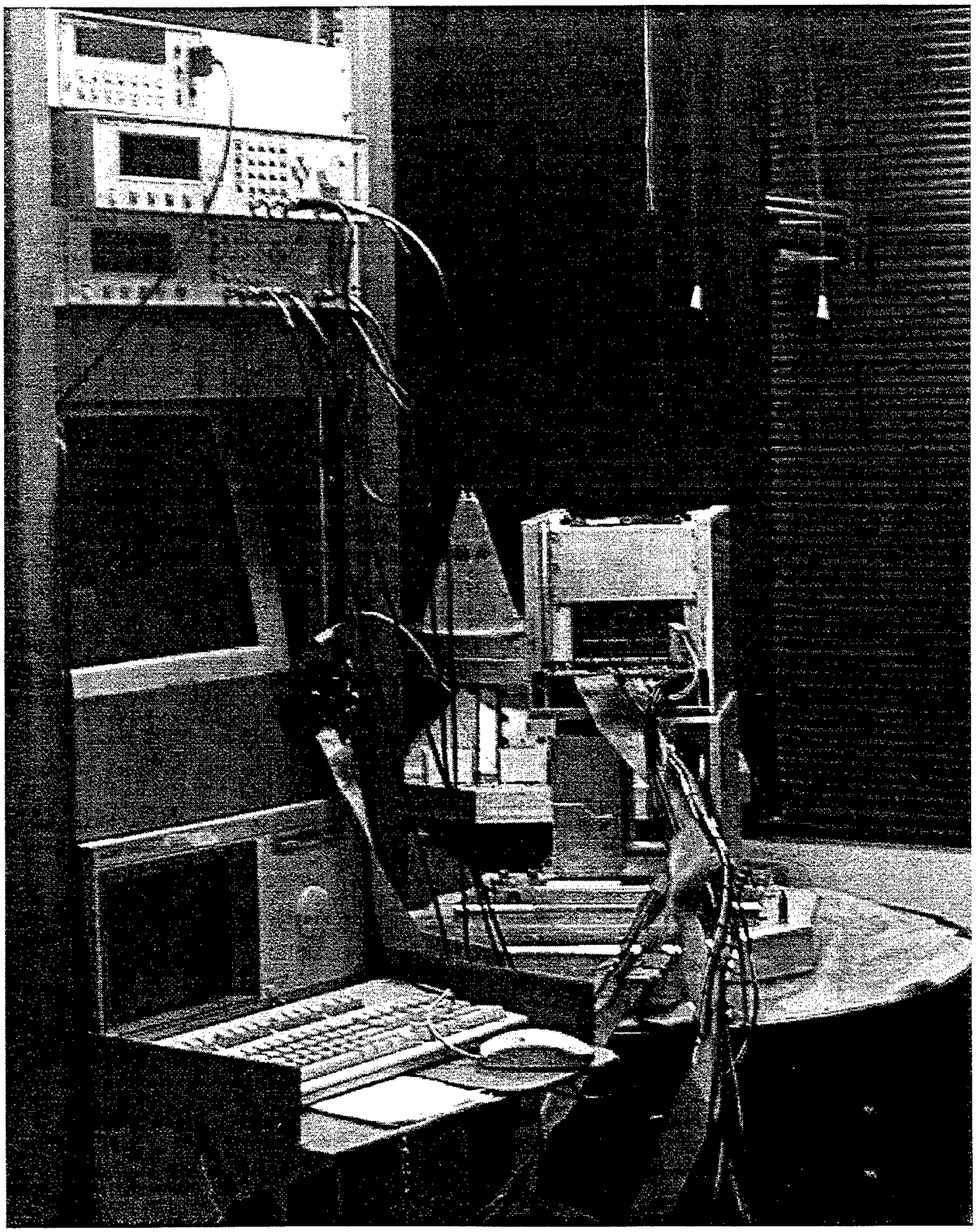


Figure 6.1.4-2 ESS Vibration Test Set-up

The results of the RF/FEC vibration testing yielded 0 failures of 44 modules built. The PNP vibration testing yielded 98.2% (1of 83 failed). This was on a Pre-PV module that

required three of the EEPROMs to be removed and replaced. The module passed on retest. Temperature cycling for the RF/FEC modules yielded 93.2% (3 of 44 failed). One failure was a differential driver that was removed and replaced. The other failure was a 5 MHz oscillator that was removed and replaced. The third failure was an MTC ASIC BIST failure. Two of the three modules were retested and both passed. The PNP modules had a temperature cycling yield of 90.4% (8 of 83 failed). One module failure was a temperature tranducer and two modules had SRAMs that required solder touch-up. After rework, the modules passed retest. Four modules had C31/DSP related failures. These are in troubleshooting. One module failed backside bus tests, and is in troubleshooting.

6.1.5 ATP/ESS Failure and Test Set Analysis

Failure analysis occurred on both the circuit cards (boards) and completed modules. ICT failure examples include a wrong or failed component, reversed diode, or improper solder connection. The test station prints out the failing node number (test point), a component number, and pin-out (ex. U17-3). From this, an examination of the component and solder joint were perfomred and board continuity was measured. Anomalies would be reworked. If no anomaly could be found, the board would be re-tested. If the same failure occurred, then the diagnosed part would be replaced. AEN has the capability of performing part removal from discretes through ball grid array packages. Rework instructions were completed by the on-line CIM system. The majority of the failures were troubleshot and repaired at AEN. Due to the complexity of the design, several boards were sent to TRW ASD for troubleshooting. Rework instructions were created at TRW ASD and the boards returned to TRW AEN for part replacement and retest. One problem associated with troubleshooting was the ability to diagnose the failure from the tester's failure documentation. In several cases, it was hard to determine where in the test the failure occurred. The printout would specify the failure, not the limits nor the tests that already passed. See Figure 6.1.5-1 below for a typical failure printout. Additional tester documentation is desired for troubleshooting.

```
BOARD SERIAL NUMBER: 097800541
U12
 (DMAD)  JX
      150113  pg-8
 Open pins.
 U12.C1  nail:39  Node: N100
  Posible fixture nail contact problem.
 U12.E1  nail:64  Node: N107
  Posible fixture nail contact problem.
U12
 (DMAD)
 150113  pg-8

 Nail   39: Pin  C1: Node: N100
 Nail   64: Pin  E1: Node: N107

BASICSCAN TEST FAILED:

OPEN OR STUCK FAILURE AT PIN(S):

C1 E1
U1
 (RTP_OPDRV)
 150111  pg-10

 Nail  106: Pin H25: Node: N137

BASICSCAN TEST FAILED:

OPEN OR STUCK FAILURE AT PIN(S):

AF17
U2
 (RTP_OPDRV)
 150111  pg-11

 Nail  105: Pin H25: Node: N136

BASICSCAN TEST FAILED:

OPEN OR STUCK FAILURE AT PIN(S):

AF17

10-AUG-98  14:52:15
 BOARD pnpb FAILED

SER #:    097800541
```

Figure 6.1.5-1 ICT Example failed Print-out

Troubleshooting at the module started with inspection, continuity, and then further diagnostic tests. Diagnostic tests were manually operated, and performed by an Engineer. Anomalies were entered in the CIM system, and recorded on the TRW ASD Events Log form. These forms are TRW ASD's required method for documenting rework to a piece of work in process hardware. Module retest followed rework. Modules that failed ASIC BIST (built-in self test) which required removal and replacement of the ball grid array package were put on hold. The ball grid array remove and replace process development was not completed for the module assemblies.

6.2 Design Verification

Design verification is performed to validate the design. Verification is accomplished by test, analysis, demonstration or inspection. Tests are run on a sample of the product and are intended to validate the design as a whole. The approach to this verification effort was to systematically address each of the requirements delineated in the Verification and Validation section of the module performance specification. For some requirements, full verification is not practical at the module level. For these, validation testing is planned as part of the military program.

Table 6.2-1 summarizes the requirements and the paragraph where the verification summary can be found.

Table 6.2-1 Requirements and Verification Summary Matrix

PERFORMANCE REQUIREMENT	B2 Req. Paragraph	B2 Appendix A Ver. Paragraph	B2 Verification Method	Summary Paragraph
LRM ELECTRICAL PERFORMANCE	3.2.7	1.1	TEST	6.2. 2
STORAGE TEMPERATURE	3.2.5.3	1.2, 1.3, 1.4	TEST IN IAR	6.2.3
OPERATING TEMPERATURE	3.2.5.3	1.5	TEST and/or TEST IN IAR	6.2.4
HUMIDITY	3.2.5.9	1.6	TEST IN IAR	6.2.5
SALT ATMOSPHERE	3.2.5.11	1.7	TEST IN IAR & ANALYSIS	6.2.6
FUNCTIONAL SHOCK	3.2.5.8.1	1.8	TEST IN IAR	6.2.7
HANDLING SHOCK	3.2.5.8.2	1.9	TEST	6.2.8
CHEMICAL /BIOLOGICAL EXPOSURE	3.2.2.6	1.10	ANALYSIS	6.2.9
BONDING AND GROUNDING	3.3.2	1.11	TEST	6.2.10
CONDUCTED EMISSIONS	3.3.2.1	1.12	TEST IN IAR	6.2.11
CONDUCTED SUSCEPTIBILITY	3.3.2.1	1.13	TEST IN IAR	6.2.11
NEAR FIELD EMISSIONS	3.3.2.1	1.14	TEST IN IAR	6.2.11
MAGNETIC SUSCEPTIBILITY	3.3.2.1	1.15	TEST IN IAR	6.2.11
RADIATED SUSCEPTIBILITY	3.3.2.1	1.16	TEST IN IAR	6.2.11
ESD SUSCEPTIBILITY	3.3.2	1.17	TEST IN IAR	6.2.12
CHEMICAL COMPATIBILITY	3.2.5.5	1.18	ANALYSIS	6.2.13
AMBIENT PRESSURE	3.2.5.2	1.19	TEST IN IAR	6.2.14
FLAMMABILITY		1.20	ANALYSIS or TEST	6.2.15
RAIN	3.2.5.10	1.21	ANALYSIS	6.2.16
FUNGUS	3.2.5.4	1.22	ANALYSIS	6.2.17
SAND AND DUST	3.2.5.6	1.23	ANALYSIS	6.2.18
EXPLOSIVE ATMOSPHERE	3.2.5.8.5	1.24	ANALYSIS	6.2.19
ACCELERATION	3.2.5.8.3	1.25	ANALYSIS	6.2.20
VIBRATION	3.2.5.7	1.26	ANALYSIS & TEST	6.2.21
WEIGHT	3.2.2.1	1.27	INSPECTION	6.2.22
RACK INTERFACE	3.2.2.2	1.28	INSPECTION	6.2.23
LRM THERMAL ANALYSIS	3.3.10	1.29	ANALYSIS	6.2.24
ELECTRICAL/ELECTRONIC HAZARDS	3.3.6.3	1.30	DEMONSTRATION &TEST	6.2.25
PERSONNEL HAZARDS & SAFETY	3.3.6.4	1.31	DEMONSTRATION, INSPECTION, AND TEST	6.2.26
MAINTAINABILITY	3.2.4	1.32	INSPECTION & ANALYSIS	6.2.27
INTERCHANGEABILITY	3.3.5	1.33	ANALYSIS & TEST	6.2.28
WORKMANSHIP	3.3.4	1.34	INSPECTION	6.2.29
MATERIALS, PARTS AND PROCESSES	3.3.1	1.35	INSPECTION	6.2.30
FINISHES & PROTECTIVE TREATMENTS	3.3.1.2	1.36	INSPECTION	6.2.31
MODULE MARKING	3.3.3	1.37	INSPECTION	6.2.32
ACOUSTIC NOISE	3.2.5.8.4	1.38	ANALYSIS	6.2.33

6.2.1 Thermal Fatigue

One of the most critical environments for the avionics modules is the exposure to long term repeated temperature cycling. Although it is not specifically addressed as a V&V

requirement in the module performance specifications, it is discussed here. This environment causes expansion stresses to occur on interconnects and other interface elements. The primary concern of these stresses is the fatigue cracking from repeated exposure to this environment. This concern was addressed early on in the design and resulted in a large investment in durability testing.

The expected life cycle temperature cycling exposure results from a combination of environmental effects and module power cycling. This exposure was analytically compressed to an equivalent number of temperature cycles of exposure for the module. This compression is a function of component temperature, materials and use environment. Compressed temperature cycles for the various PBGA solder joints used on the IBP-MPCL programs ranged from 800 to 1500 cycles for a cycle of –45°C to 95°C. For final verification, two of each PV module type were exposed to a full equivalent lifetime of temperature cycling.

An FEC design deficiency was uncovered when temperature cycling caused cracked solder joints on two RF switches on the B board (SW-313). A design change was implemented to resolve this issue. This design change meets the life requirement analytically. All other components passed electrical performance tests after exposure.

The PNP passed all electrical performance tests after exposure to an equivalent lifetime of temperature cycling.

6.2.2 LRM Electrical Performance

The IBP-MPCL Performance Specifications (B2 Specs) contain matrices to verify the LRM Electrical Performance per the tests stated in the verification section paragraph 1.1. The electrical performance requirement was verified by successful completion of the ATP for the PNP and FEC.

6.2.3 Storage Temperature

Storage temperature testing was performed on an FEC and a PNP. Each module was subjected to the storage temperature environment required in the IBP-MPCL performance specification. Each module passed ATP after exposure to this environment. This requirement has been successfully met.

6.2.4 Operating Temperature

This requirement is considered verified by successful completion of ESS temperature cycling. Each of the deliverable PV modules received 10 ESS cycles. SBIT is operated over temperature from –40°C to +60°C.

6.2.5 Humidity

Testing was performed to the test procedure in the performance specification for both the PNP and FEC module. Post test inspection showed no physical damage. Post test ATP of the PNP was successful. Post test ATP of the FEC indicated a DSP ASIC failure. The DSP in question had an I/O failure, in which the Backside Bus Data 13 line appeared to be stuck in a tri-state mode.

A failure analysis was conducted to determine if the cause of the failure was related to moisture intrusion during the humidity test. Decapsulation of the DSP and SEM examination of the die near the I/O location in question did not reveal the presence of any corrosion or corrosion by-products. Moisture intrusion was not the likely cause of the failure. Further analysis (die-level deprocessing) would be required to determine the actual cause of the failure.

6.2.6 Salt Atmosphere

Extensive development testing was performed that exposed DV hardware and test vehicles to corrosion testing in a salt atmosphere.

A 500 hour salt fog test per MIL-STD 810E (35°C, 5% NaCl solution) was conducted on two of the fully populated Component Reliability boards (CR1). Both boards were functionally tested before and after the 500 hour exposure. In both cases, all the microcircuit devices on both boards remained functional after the salt fog test.

The photographs shown in Figures 6.2.6-1 through 6.2.6-3 show CR1 test circuit board 6C before and after the 500 hour salt fog test. Figure 6.2.6-2 shows the board just as it looked when removed from the test chamber. A deionized water rinse was performed and the results are shown in Figure 6.2.6-3. The board was resubmitted to functional testing and passed.

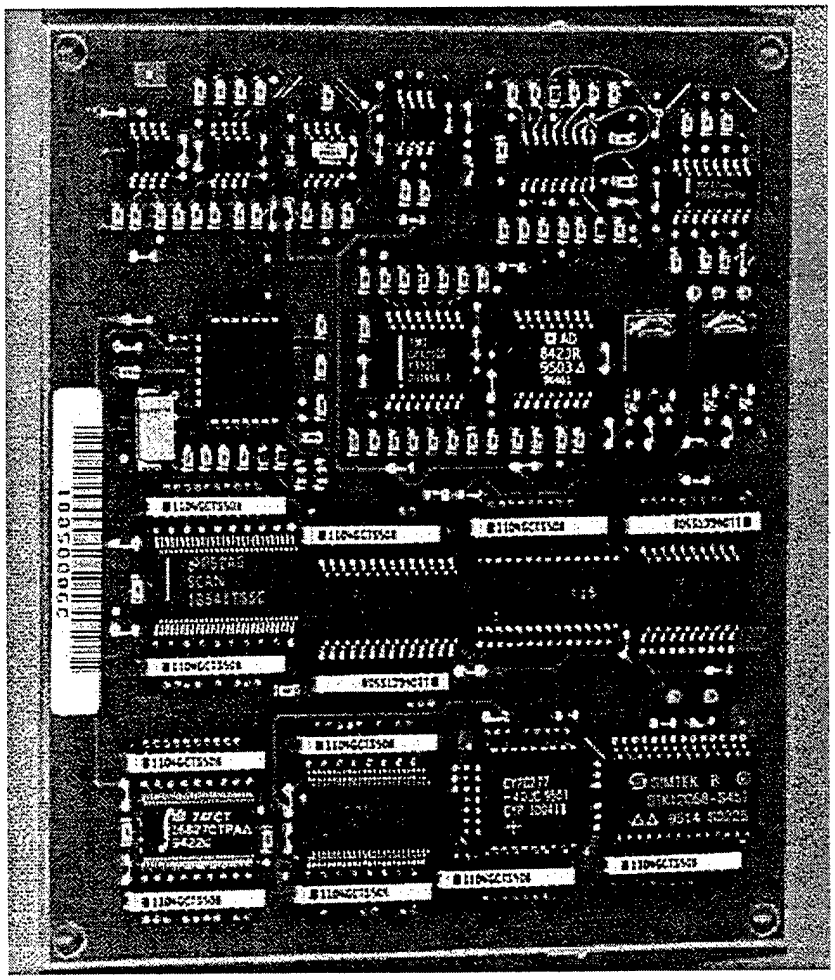


Figure 6.2.6-1 CR1 Board 6C, Prior to 500hour Salt Fog Test

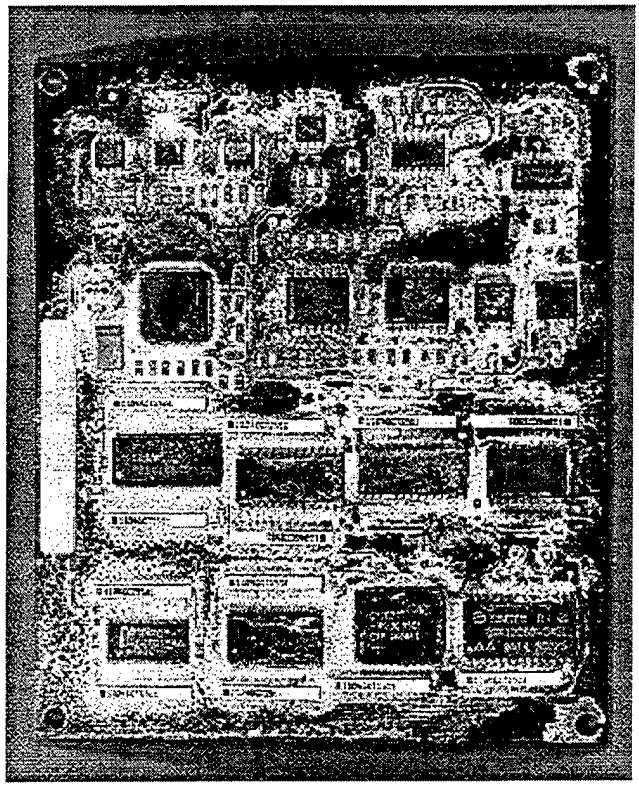


Figure 6.2.6-2 CR1, Board 6C, Post 500hour Salt Fog Test.

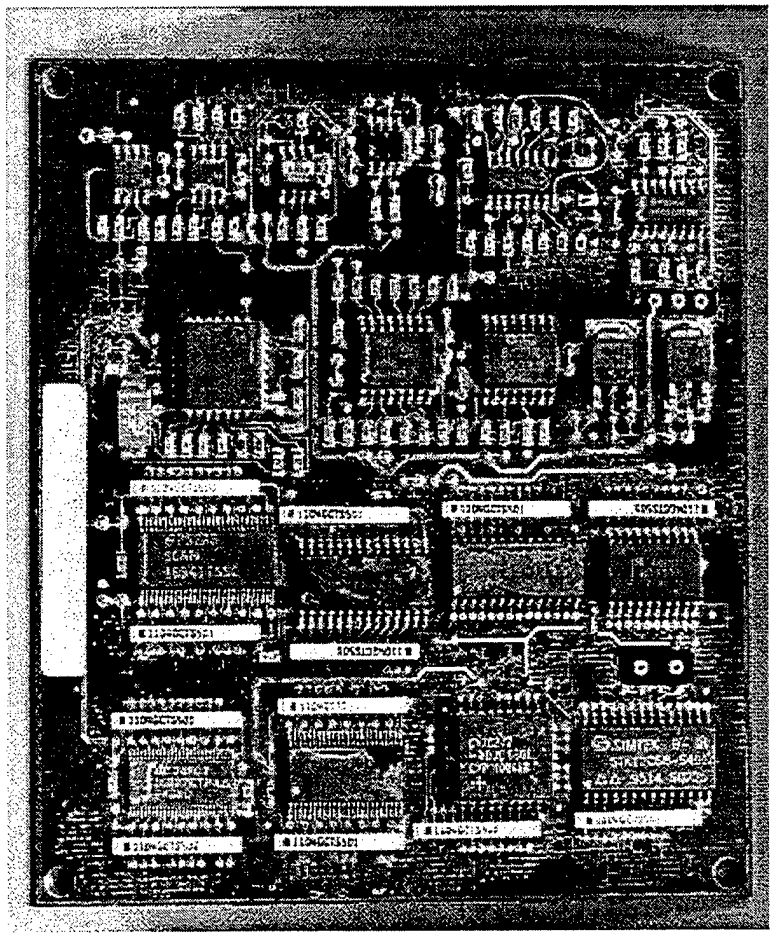


Figure 6.2.6-3 CR1, Board 6C, Post DI Rinse, Post Salt Fog

Figure 6.2.6-4 shows a portion of the DV core cover combination after exposure to the 500 salt-fog environment. Evidence of this corrosive damage led to the decision to redesign the cores and covers for PV.

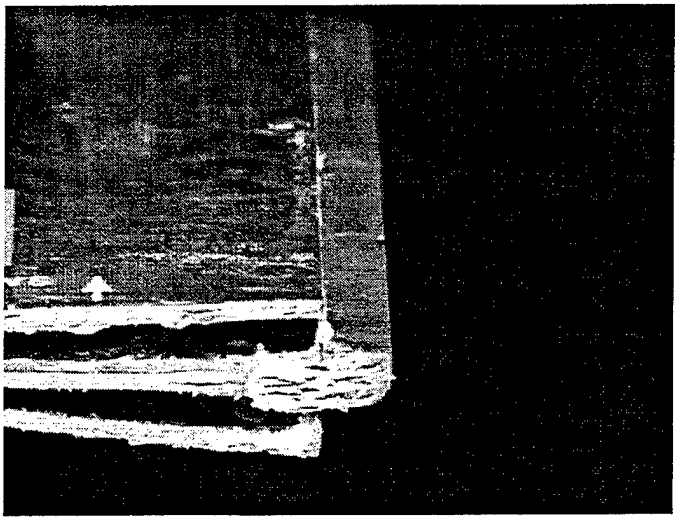


Figure 6.2.6-4 DV Core and Cover After Salt Fog Exposure

The information learned from this testing helped drive design decisions for the hardware. There was no verification testing performed on the PV hardware in its final state. Verification to this requirement is based on the results of development tests and the fact that customer approved protective finishes and platings were used on all surfaces that will be exposed to corrosive environments.

6.2.7 Functional Shock

Functional shock testing was not performed. It is expected to be less severe than the module vibration exposure and enveloped by vibration testing.

6.2.8 Handling Shock

Testing was performed to the Bench handling test procedure described in the performance specification. The specification states that drop height will be 4 inches, 45°, or the point of balance, whichever is less. In the case of the module, the 4 inch drop height was used. Post test inspection showed no damage and post test ATP showed no functional degradation. The module design can be considered qualified to this environment.

6.2.9 Chemical / Biological Exposure

No analysis was performed. Materials and finishes selected conform to the customer furnished selection guidelines. This environment is not believed to be a design driver. Chemical Environmental exposure is likely to have identical impact to the military hardware replaced.

6.2.10 Bonding and Grounding

Miliohmeter measurements were performed on cover/core combinations. The PV covers met the requirement for the connector to core interface, but were above the acceptable tolerance for the cover to cover measurement (15 mΩ versus the required 2.5 mΩ). The 15mΩ reading was accomplished with a different set of probes, and a good connection could not be obtained. This is not believed to be an impact to the modules bonding and grounding ability.

6.2.11 EMI

Cover shielding effectiveness tests were performed on the 6 cover styles shown in Table 6.2.11-1. Testing occurred at two facilities that required the resultant data to be normalized. The covers were tested over the frequency range of 50 KHz to 18 GHz . The military contract's AlBeMet cover was used as a control to determine chamber differences, antenna placement, and aperture differences. Both facilities used a transmitting antenna in an anechoic chamber, but the second test facility received in an unshielded room. The covers were bolted to an IBP-MPCL module core that had a 4.2" x 4.4" aperture removed from the center. Conductive tape was used to cover the gap on the connector and top end of the mating surfaces. The sides were left untaped between the core and the cover, representing a "normal" leak path. Figure 6.2.11-1 and 6.2.11-2 show pictures of the test set-up.

Figure 6.2.11-3 indicates that the GFRP reference plate (PV cover without shielding) was not acceptable in producing 40db of shielding effectiveness. Military's AlBeMet was capable of meeting this requirement. The Cad/Ni plated version of the PV cover exceeds this requirement and was used for the PV design.

Table 6.2.11-1 Cover Configurations used for EMI Testing

	Materials	**Plating**	**Paint**
Military Baseline	AlBeMet	Cad/Ni	Epoxy
IBP-DV	Gr/Epoxy and Al	None	None
IBP-PV Ver. 1	Gr/Epoxy	None	None
IBP-PV Ver. 2	Gr/Epoxy w/ nickel mesh inside	None	None
IBP-PV Ver. 3	Gr/Epoxy w/ nickel mesh outside	None	None
IBP-PV Ver. 4	Gr/Epoxy	Cad/Ni	None

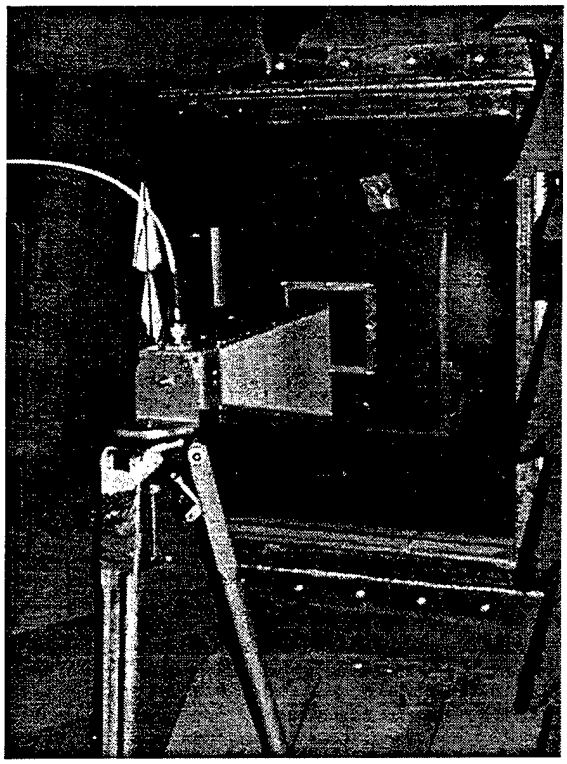


Figure 6.2.11-1 Chamber Setup, High Frequency Measurements

Figure 6.2.11-2 Chamber Setup, Low Frequency Measurements

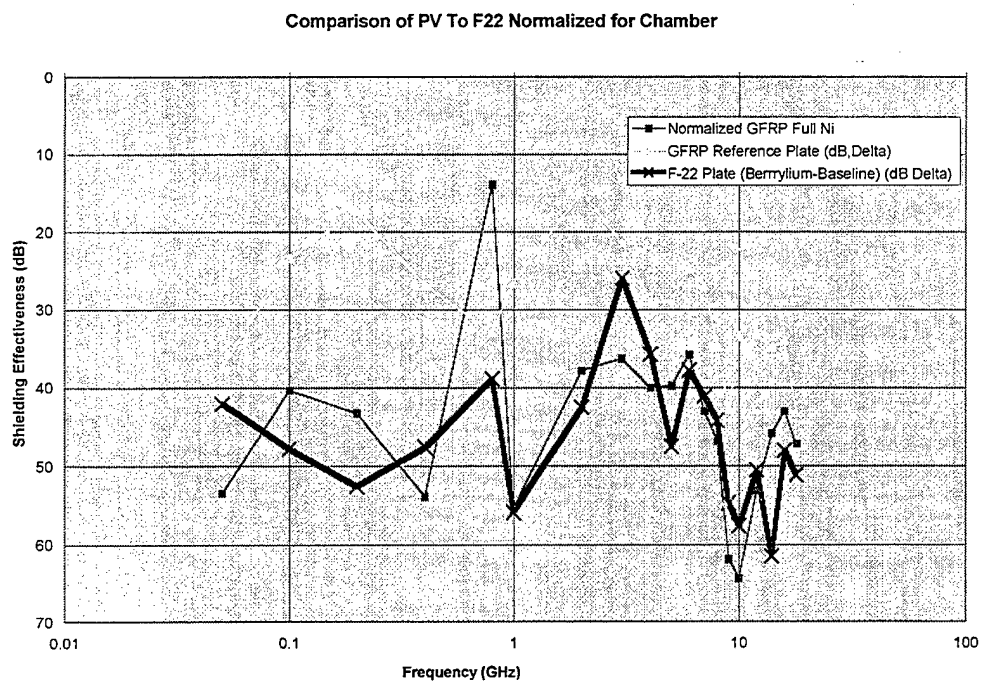


Figure 6.2.11-3 Comparison of Shielding Effectiveness

6.2.12 ESD Susceptibility

No testing was performed on the IBP-MPCL modules for this requirement. From a design standpoint, the ESD protective circuitry is the same as the military modules. Testing would be expected to yield similar results. The backplane connector which is a customer defined component common to both designs, successfully passed ESD testing. It is the primary ESD shielding mechanism of the module.

6.2.13 Chemical Compatibility

No analysis was performed. Materials and finishes selected conform to the customer provided selection guidelines. This environment is not believed to be a design driver. Fluid exposure to water, detergents, solvents, oils, fuel and refrigerants is likely to have identical impact to the military hardware replaced.

6.2.14 Ambient Pressure

Pressure testing was performed per the test procedure without LRM power applied. No damage was noted on the modules and each module passed full electrical testing after exposure to this environment. Full pressure testing with the modules powered will be performed as part of safety of flight testing at the IAR level.

6.2.15 Flammability

No analysis was performed. Materials and finishes selected conform to the customer provided selection guidelines. This environment is not believed to be a design driver. The IBP-MPCL LRM does not contain flammable materials and is likely to self extinguish in the 5 minute period allowed.

6.2.16 Rain

No analysis was performed. Materials and finishes selected conform to the customer provided selection guidelines. The rain environment is believed to be enveloped by the corrosion test environments. Significant moisture testing or analysis has been performed on all IBP-MPCL components to verify absence of performance degradation.

6.2.17 Fungus

No analysis was performed. Materials and finishes selected do not support fungal growth. Fungal environment is not believed to be a design driver. Exposure is likely to have identical impact to the military hardware replaced.

6.2.18 Sand and Dust

No analysis was performed. Materials and finishes selected conform to the customer provided selection guidelines. The sand and dust environment is not believed to be a design driver. Sand and dust exposure is likely to have identical impact to the military hardware replaced, as identical backplane connectors are used. Covers, metal finishes, or conformal coatings protect all other surfaces.

6.2.19 Explosive Atmosphere

The objective of this analysis was to verify that the LRMs could be installed, operated and removed in a flammable atmosphere with out explosion or ignition. Parts lists of each module were reviewed and no capacitors or accumulators of static electricity were found sufficient to cause arcing or ignite an explosive atmosphere. Thermal analysis shows that worse case component temperatures are well below the ignition temperature of N-hexane (222.8°C)

6.2.20 Acceleration

An analysis was performed that showed that X axis vibration loads are more severe than loads imparted due to acceleration. In plane acceleration loads are shown to be orders of magnitude below the material capabilities.

6.2.21 Vibration

This environment causes stresses to occur on interconnects and other interface elements. The primary concern of these stresses is the fatigue cracking and failure that can result from exposure to this environment. This concern was addressed early on in the design and resulted in a large investment in durability testing.

For final verification, the aircraft environmental requirement was modified by the rack transmissibility to determine the expected module level input. The duration of exposure was determined by analytically compressing the life cycle vibration environment to an equivalent test duration in each axis. An FEC and a PNP module were subjected to the equivalent life test. Post test inspection of the modules showed no damage. Post test ATP of the modules was successful.

6.2.22 Weight

The modules were weighed on a calibrated scale and are compliant to the maximum weight of the specification. The PNP weighed 1.02 pounds and the FEC 1.03 pounds.

6.2.23 Rack Interface

A comparison of the module build package was compared to the interface control drawing for the modules. The ICD requires a minimum corner chamfer of 0.35 in. on the module B covers. The design uses a chamfer of 0.25 in. The 0.35 requirement is understood to have been incorporated due to an obsolete design for the inserter/ejectors. This non-compliance does not create any interference or impediment to the use of the module in the rack.

6.2.24 LRM Thermal Analysis

The LRM thermal analyses are discussed in detail in section 4.3.3.3 of this report. The analysis shows a specific non-compliance with the stated requirement that all junction temperatures remain below 105°C. The PNP B DMAD is shown to have a junction temperature of 105.7°C. This noncompliance is not expected to adversely effect the reliability of the module. There is an additional requirement that the thermal analysis match measured data within 5°C. The thermal analysis was compared to infrared images of the modules in the test set. The IR images were used to estimate case temperature under the same interface conditions as the thermal analysis performed. The comparison showed that the results were within ±10°C from the expected temperatures. The analysis was not "re-tuned" to match the measured data.

6.2.25 Electrical/Electronics Hazards

Voltage measurements have not been made between the Integrated Avionics Rack (IAR) and the external LRM surfaces to verify ground potential during power up. It is highly likely that the design will pass these tests when they are run.

Power is manually removed before installing, replacing or interchanging the LRM and is demonstrated by rack integration of numerous IBP HWCIs.

The LRM can not be physically mismated to the Integrated Avionics Rack (IAR) as it is protected by backplane and module "keying" and as demonstrated by IAR fit check.

The LRM can be physically mismated to the test sets that have common backplane connectors as these test sets are not yet "keyed".

6.2.26 Personnel Hazards and Safety

The LRM and Backplane (IAR) connectors are designed with equivalent voltage rating. The LRM contacts are all socket type contacts, except the ESD pin, which is at ground potential. External surfaces of the module are at ground potential. Power can be manually removed from the module for removal, interchange or replacement.

Any potential LRM failure mode will not result in hazardous electrical shock or physical injury to test and maintenance personnel.

6.2.27 Maintainability

Modules with fasteners were subjected to durability life testing with no evidence of failures.

The fasteners used for the covers are self-locking and are good for up to 5 removal and replacement cycles. Loctite is used on the fasteners to provide additional support. On-aircraft fault isolation and field troubleshooting will not require LRM cover removal. Cover removal will be conducted at the depot level where the fasteners will be removed and Loctite will be reapplied following any rework/repair of the LRM.

6.2.28 Interchangeability

The components selected for the PNP and FEC LRMs do not require any adjustment or tuning to be used on a given circuit card assembly. There are no LRM level select-in-test operations that would require the use of different component part numbers for a single CCA part number.

6.2.29 Workmanship

Visual examination of every HWCI was performed prior to conformal coat for verification of these requirements. Non-conformances were reworked to conform.

Components and the assembled LRM module are free of smudges, loose, spattered, or excess solder or any foreign material that might detract from the intended operation. The printed wiring boards show no evidence of burning, blistering, or delamination. No PTHs are soldered. Mechanical fasteners show no evidence of cross threading, mutilation, or detrimental or hazardous burrs, and are secured by torque level, thread lock compound, and locking helicoil in some cases.

Wires and cables are positioned or protected to avoid damage to conductors or adjacent components.

Part markings and reference designations are legible and conform to print, and components are mounted in such a manner that markings are visible. Chip resistors are mounted with the resistive element away from the printed circuit board

Leads on opposite sides of surface mounted flatpacks are formed such that the non-parallelism between the base surface of the component and the surface of the printed wiring board is minimal.

Lead bends of surface mount devices do not extend into the body of the device. The lead bend radius is greater than or equal to the nominal lead thickness. The angle of that part of the lead between the upper and lower bends in relation to the mounting land is 60 to 90° maximum.

Component package bodies do not show evidence of damage due to lead deformation. The top of the leads do not extend beyond the top of the package body.

Soldered connections conform to the General Requirements of ANSI/J-STD-001, Section 9.2, except as defined separately in IPC-610. Hardware was inspected to IPC-610 class 3 requirements.

Conformal coating conforms to the General Requirements of ANSI/J-STD-001, Section 10.0, except as separately defined in the assembly prints.

6.2.30 Materials, Parts and Processes

The modules have no dissimilar metals in contact with each other. Encapsulating materials are hydrolytically stable and removable. Encapsulating material, thermal core and cover plating have been tested and do not crack, chip, or peel. The cards are tested to 500V and per UL specification, are capable of 1000VRMS 60Hz for 1 minute between terminals without arc.

Parts selected meet the HWCI performance, integrity, durability and reliability requirements. Parts used beyond manufacturer's recommended limits were tested or analyzed to be most effective in trades of cost, integrity, and circuit performance.

Silicone conformal coat is applied to the LRM at a thickness of 0.005 to 0.008 in. There are no hard-anodized aluminum surfaces. Thermal rails are Cadmium over Nickel plated to match the IAR surface. The non-bearing surfaces of the module covers are black chromate conversion of Cadmium plate. The thermal core transfer surface finish specified is 32u and flat to 0.005" after plating.

6.2.31 Finishes and Protective Treatments

The LRM thermal rails as measured do not meet the 32u surface finish requirement. These measurements were performed on LRM's after numerous insertion/extraction cycles, and abrasion with the test adapters may contribute. The thermal core base material is a graphite lay-up that is cured under pressure. The tool surfaces control the surface finish, and meet the 32u requirement. The thermal core is activated for plating with chemistry that etches this surface. Etching and lack of plating uniformity will reduce the surface finish. Engineering review of the resulting surface indicates that it is still acceptable for use.

Conformal coating conforms to the General Requirements of ANSI/J-STD-001, Section 10.0, except as separately defined in the assembly prints. The connectors are not coated. Masked areas are identified per the print. By drawing, the thickness of the coating is 0.005 to 0.008". The coating is free of voids, blisters, and delamination except at the interface with BGA underfill, where these features are allowed.

6.2.32 Module Marking

LRM marking conforms to all requirements except for the placement of a four digit key code on the module end surface. This information is placed on the cover top surface only, and omits the two digit alpha code (4 numeric only). The markings are permanent, do not violate the 0.580" overall module thickness, and conform in height and color to all requirements.

6.2.33 Acoustic Noise

An analysis was performed that showed that the module response to the acoustic environment is less severe than the acceleration environment. The module can be considered validated to this environment based on validation of the acceleration environment. Other effects of acoustics such as structure borne vibration are considered to be enveloped by the vibration requirement.

7.0 PROGRAM GOAL SUMMARY

IBP-MPCL achieved or exceeded program goals. The positive impact of this program has changed the processes used to design and build military avionics at TRW ASD and the military business posture of TRW AEN. The program's "demonstration" of a commercial line's capability to produce military electronics evolved into a pilot program that fielded and delivered flightworthy SEM-E modules to the Air Force and the Army.

7.1.1 Quantitative Results

Tangible and quantitative results were achieved on IBP-MPCL. As a demonstration program, pilot and deliverable hardware were produced. The program built 187 SEM-E modules for test, evaluation and delivery. Test hardware to support component reliability testing and durability analysis for these modules included 200 circuit card assemblies, 50 test modules, and 4000 components.

PNP module recurring costs were reduced 48% and the RF/FEC module 70% as demonstrated by procurement of the BOM, assembly and test. Design verification tests, acceptance tests, and use of the hardware in the integrated avionics rack verified module functionality. Durability life tests on multiple specimens verified hardware robustness. Measurements on the PNP and the RF/FEC demonstrated 30 and 32% weight reductions respectively.

TRW AEN demonstrated 15-minute manufacturing line conversions from commercial product, to military product, and return. Process capabilities were measured for dominant processes on the hardware produced to demonstrate capabilities (Cpks) in excess of 1.33.

7.1.2 Qualitative Results

A measure of program success is duplication. TRW ASD has commenced work on conversion of other military electronics using the principles and concepts of the IBP-MPCL program. This hardware will all be produced at TRW AEN-Marshall.

Additional TRW ASD military designs are utilizing the dual use methodologies developed on IBP-MPCL for part selection and product design. TRW ASD has gained a competitive advantage for lower cost military electronics that customer's demand.

As a consequence of the IBP-MPCL demonstration, TRW AEN has gained valuable process technology, acquired new infrastructure, and substantially increased its business potential for manufacturing military hardware.

The military has benefited from lower cost military electronics, receipt of demonstration hardware, and development of the commercial base, for nominal or surge capacity, as a viable source of supply.